APPLICATION ASPECTS

5.1 Gate Drive Considerations

Introduction

The main purpose of a gate driver for a phase control thyristor (PCT) is to provide a gate current of the right amplitude, at the right time, and of the right duration. This would seem simple, but the analysis of failed thyristors due to inadequate gate pulses leads to the conclusion that the proper design of a gate drive unit is not trivial. This section points out some of the most important gate drive design rules.

Current or Voltage?

A thyristor is a *current*-controlled bipolar semiconductor, unlike MOS-FETs or IGBTs which are *voltage* controlled. Therefore, a thyristor gate drive unit is primarily a *current* source, supplying a specifically shaped current pulse from gate to cathode. The voltage drop along the gate-to-cathode path is a function of the gate current and the internal impedance between gate and cathode. For this reason, a thyristor manufacturer specifies gate *current* levels rather than gate voltage levels.

Gate Current Requirements

In this note we will focus on gate drive requirements for general applications; for special load conditions like e.g. pulsed power switching, ABB Semiconductors' application engineers should be consulted.

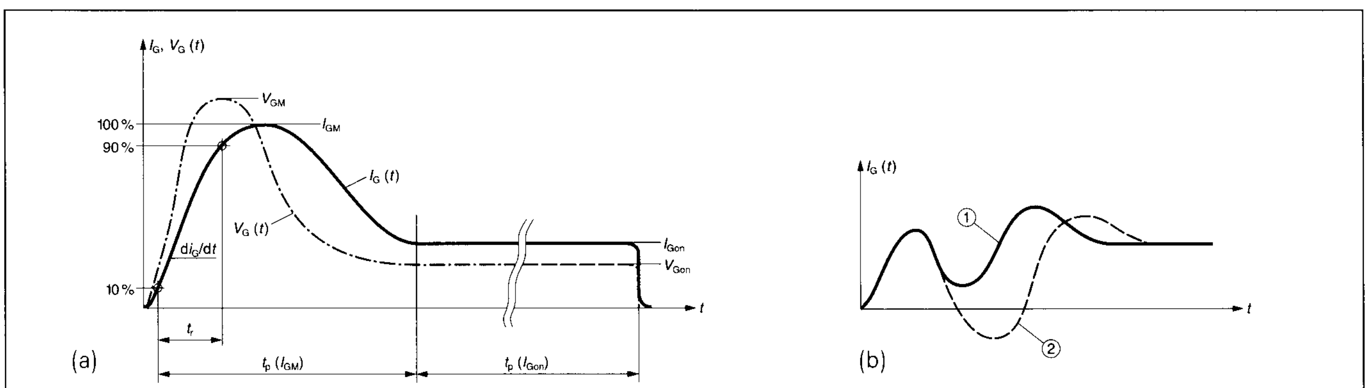

Fig. 1
a) Current and voltage waveforms of a typical gate pulse as recommended for general applications with PCTs.
b) Distorted gate current waveforms as a result of a weak gate driver with too low supply voltage.
(1) Medium distortion
(2) Severe distortion

Fig. 1 a) depicts a gate current pulse suitable for most applications. The current wave-shape and its characteristic parameters will be discussed and typical values will be given so that a gate unit can be optimised for specific applications.

- *I_{GM}, di_G/dt, t_r and $t_p(I_{GM})$*

These parameters specify the initial part of the gate pulse. They strongly affect the following thyristor characteristics and ratings:

- Turn-on delay time
- Turn-on fall time of the anode voltage
- Turn-on switching energy
- Critical di/dt of the anode current at turn-on

A high I_{GM} and a low t_r, i.e. a high di_G/dt, enhance all of these ratings and characteristics. This is of particular importance in the following cases:

1. *High Turn-On di/dt:* A strong initial gate pulse ensures that the amplifying gate and the main gate are fired homogeneously. A weak gate pulse is dangerous for the sensitive gate structures since a local gate current flow results in a local anode current flow. This in turn can lead to a hot-spot with subsequent device failure.
2. *Series Connected Thyristors:* At turn-on, it is important that all individual devices turn on simultaneously, otherwise the slower devices may be subjected to over-voltage. In order to minimise the differences in delay times, Δtd, within a stack of series connected PCTs, the delay time td itself must be minimised by the application of a strong gate pulse. Small imbalances in the turn-on transition, which will always be present because of manufacturing scatter and slightly different junction temperatures, can be controlled by connecting an RC snubber circuit in parallel. The RC snubber is needed in most applications anyway to limit voltage overshoot at turn-off.
3. *Parallel Connected Thyristors:* Imbalance in the turn-on characteristics of parallel connected thyristors is minimised by a strong gate pulse. This is important for good current sharing during the dynamic turn-on phase.
4. *Thyristors Operated in Electrically Noisy Environments:* This may necessitate a noise filter between gate and cathode which will further weaken the gate pulse.

Recommended values for I_{GM}, di_G/dt, t_r and $t_p(I_{GM})$ for all PCTs from ABB Semiconductors are:

I_{GM}	$\approx 2 \ldots 5$ A
di_G/dt	$\geqslant 2$ A/µs
t_r	$\leqslant 1$ µs
$t_p(I_{GM})$	$\approx 5 \ldots 20$ µs

I_{GM} should not exceed 10 Amperes, as indicated in the data sheet (I_{FGM} rating). For di_G/dt, there is no upper device limit, i.e. the gate current rise rate is only limited by the driving voltage and gate lead inductance (see also discussion of V_{GM} parameter below).

The duration of the gate current overshoot, $t_p(I_{GM})$, should be in the range specified above; 5 µs are sufficient for an anode current di/dt ⩾ 20 A/µs, and 20 µs would be adequate for di/dt ⩽ 5 A/µs.

- I_{Gon}

In a variety of applications, the instant at which the anode voltage becomes positive and the thyristor has to take over the load current cannot be synchronised with the gate driver. In this case a so-called "back-porch current" (I_{Gon}) is provided to trigger the thyristor as soon as the anode voltage becomes positive. Because the ensuing di/dt of the anode current is low, it is sufficient to keep I_{Gon} slightly above the minimum gate trigger current, I_{GT}, for the specified minimum junction temperature.
This back-porch current is also indispensable in those cases where the anode current is subject to uncontrolled changes and can fall to values close to the holding current, I_H, or even become negative. I_{Gon} then ensures that the thyristor remains turned on during the whole intended conduction period.
The influence of I_{Gon} on the on-state voltage V_T is negligible unless the anode current is extremely low, i.e. close to the holding current.
It is recommended to use a back-porch current, $I_{Gon} \geqslant 1.5 \cdot I_{GT}$ where I_{GT} is the specified gate trigger current at the minimum expected junction temperature.

- $t_p(I_{Gon})$

The duration of the back-porch current must be long enough to ensure that the thyristor is able to trigger at any time in the prospective conduction period, as discussed above (I_{Gon} parameter).
$t_p(I_{Gon})$ is determined by the load conditions; no general values can be specified. However, *care must be taken that $t_p(I_{Gon})$ is not too long,* as explained at the end of this sub-section ("Applying Positive Gate Current During Reverse Blocking").

- V_{GM}

At the beginning of this section, it was stated that the gate voltage is the reaction of the thyristor to the applied gate current. In the first phase of the turn-on process, the gate-to-cathode impedance is higher than the steady-state value given in the data sheet (V_{FG} vs. I_{FG} characteristic). The dynamic gate voltage is a function of the charge carrier concentration in the gate region, the internal inductances and, last, but not least, the di/dt of the anode current. With a gate pulse as specified at the beginning of this sub-section, the peak gate voltage V_{GM} can reach amplitudes of 12 Volts or even more. This has to be considered when the supply voltage source for the gate pulse amplifier and the gate pulse transformer are designed. If the open-circuit gate drive voltage is too low, the gate current may be considerably distorted, as depicted in fig. 1b). Curve (1) illustrates a medium distortion where I_G (t) has an instantaneous minimum close to zero, and the dashed line (2) shows a severe distortion where I_G (t) briefly becomes negative. Both cases shown in fig. 1b) are dangerous for the thyristor and may lead to failure. In this context it is recommended that the design of the gate unit allow for gate current measurements under worst-case conditions (max. anode di/dt), where possible. During measurements performed in our laboratory with a weak gate driver, "proper" waveforms as shown in

fig. 1 a) were obtained with the anode (main) circuit disconnected, but as soon as a certain di/dt was applied, the wave-shape became distorted per fig. 1 b).
A gate drive supply voltage of ⩾ 20 V for moderate di/dt applications and ⩾ 30 V for high di/dt requirements is recommended.
In order to minimise the inductance of the gate lead, it is advantageous to mount the gate driver as close as possible to the thyristor and to twist the gate leads or to use coaxial cables. Care must be taken that the gate leads not be exposed to any surfaces at high potential or to fast changing magnetic fields in order to avoid electromagnetic disturbances or even flash-over to the gate leads.

Applying Positive Gate Current During Reverse Blocking

When the thyristor is in its reverse blocking state, there is no risk of *triggering* by a positive or negative gate current. However, applying reverse anode voltage and positive gate current simultaneously is still dangerous for another reason.
Due to transistor action, the reverse leakage current I_R increases drastically above its nominal value when I_G is positive; low gate currents below 1 A can provoke leakage currents of several 100 mA even at room temperature. Besides additional power losses, this operation can lead to device failure and must be avoided under all circumstances. This should be considered when defining $t_p(I_{Gon})$.

5.2 Design of the RC Snubber Circuit

To protect a thyristor against over-voltages during the turn-off process, it is common to use an RC snubber circuit as shown in fig. 2. If many thyristors are connected in series, every thyristor normally has its own RC snubber.

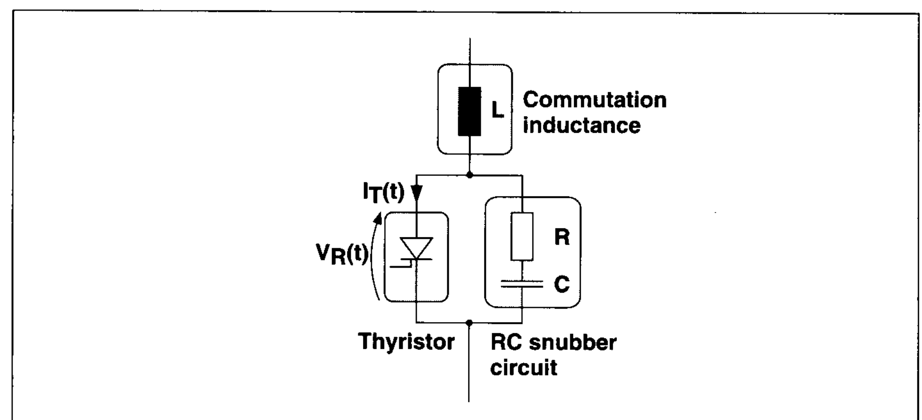

Fig. 2
Typical PCT circuit with RC snubber and commutation inductance.

The voltage transients typically occurring across the thyristor during turn-off are displayed in fig. 3.

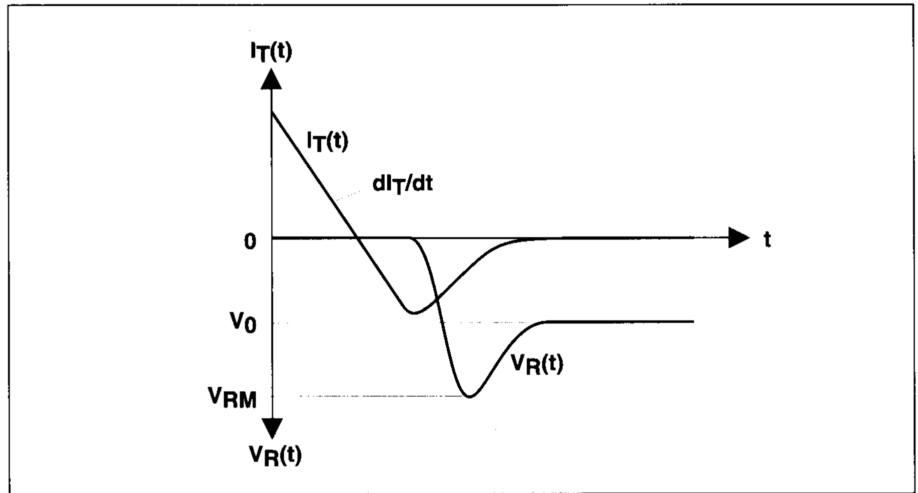

Fig. 3
Typical voltage and current waveforms during turn-off.

The voltage utilisation of the thyristor is given by V_0, but the voltage peak value, V_{RM}, during turn-off must not be exceeded. It is therefore useful to keep a low ratio of V_{RM}/V_0 with an appropriate snubber design. A small capacitor will save cost and losses. The curves in fig. 4 serve to optimise the choice of R and C.

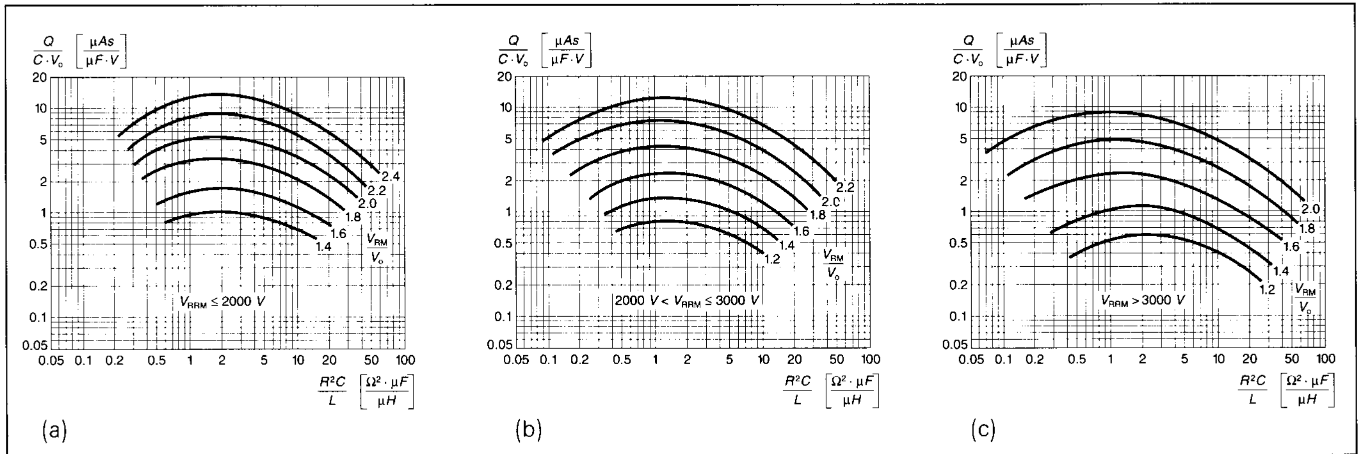

Fig. 4
Curves for determining the optimal RC snubber values. The curves in (a), (b) and (c) are valid for thyristors with V_{RRM} ratings below 2000 V, between 2000 and 3000 V and above 3000 V.

The procedure for designing a snubber is as follows. It is assumed that the stationary voltage V_0 and the commutation inductance L are known. The ratio V_0/L then gives the current fall rate di_T/dt. From the thyristor data sheet we read the Q value at this di_T/dt. Knowing the desired ratio V_{RM}/V_0, the minimum capacitor C can be found by reading $Q/C \cdot V_0$ at the maximum of the curve in fig. 4. Since C and L are known, reading the value $R^2 \cdot C/L$ on the horizontal axis then yields the value of R.

Example:
A 5STP 25L5200 is to be used at $V_{RM} = 3200$ V and $V_0 = 2000$ V: V_{RM}/V_0 is therefore 1.6. The commutation inductance is 100 µH, so that di_T/dt is 20 A/µs. The data sheet shows that the maximum Q at 125 °C is

$15000\,\mu As$. From fig. 4 c) the optimum value for C, corresponding to $Q/C \cdot V_0 = 2.4\,\mu As/\mu F \cdot V$, is found to be $C = 3.13\,\mu F$. From the horizontal axis of fig. 4 c), $R^2 \cdot C/L = 1.4\,\Omega^2 \cdot \mu F/\mu H$ and thus $R = 6.7\,\Omega$. The standard values $C = 3.3 \mu F$ and $R = 6.8 \Omega$ are retained.

5.3 Housing with Enhanced Explosion Ratings

ABB Semiconductors has developed an explosion-resistant housing alternative to the N-type housing primarily for paralleling devices in high current rectifier applications.

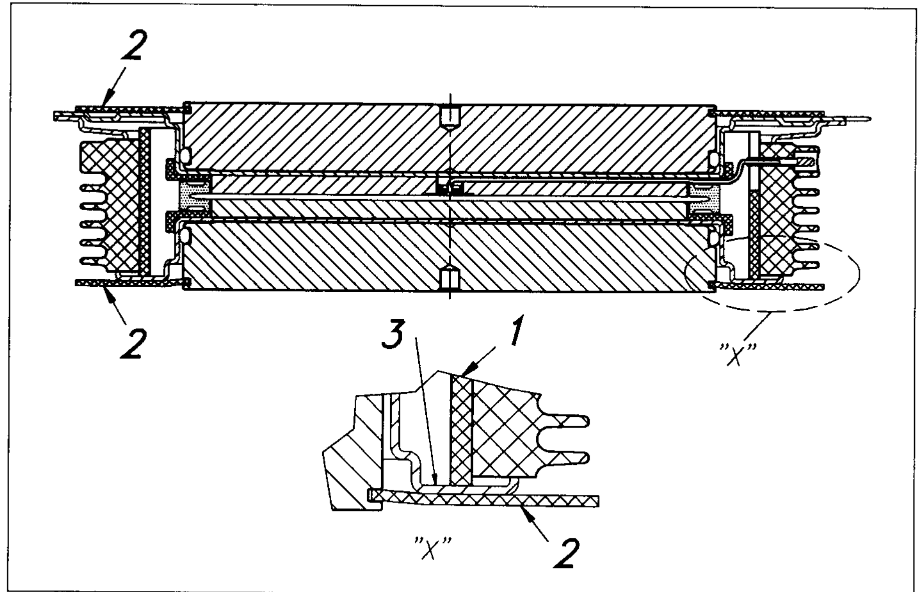

Fig. 5
Basic design of an explosion-resistant press-pack housing.
1 Inner protection shield (silicone rubber)
2 High density polyethylene ring
3 Destruction point at flange

The housing ceramic is re-enforced with an inner protection which acts as a heat absorber and shield for thermal shocks occurring during short-circuit conditions. This inner buffer protects the ceramic ring and directs the over-pressure to the flange where a hole is created when the explosion integral is exceeded.
The material chosen for this inner buffer is a silicone rubber strip. The heat sink opposite the housing flange is shielded from the ensuing arc with a high-density polyethylene ring. The worst-case explosion-integral occurs when a thyristor fails in the reverse direction as this produces the highest short-circuit device resistance and thus the highest energy dissipation (see fig. 6).

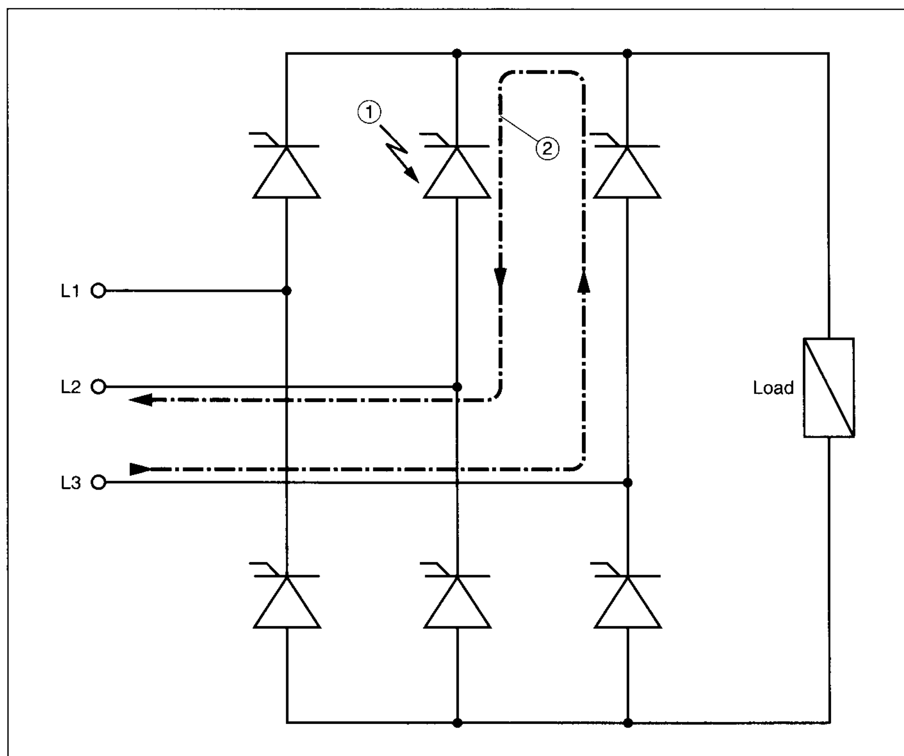

Fig. 6
Basic circuit configuration for worst-case explosion condition.
1 Shorted thyristor (reverse direction)
2 Short circuit current path

This worst-case failure mode is used for testing and designing.
Both the explosion-resistant N-type housing and the standard N-type housing withstand single surges of up to 90 kA at t_p = 10 ms without rupturing.

For the explosion-resistant design, two failure modes are of interest: circuits with and without fuses.
In unfused circuits with prospective surge currents above 90 kA, the heat shock is so great that the ceramic ring may crack. This failure mode is not explosive as the inner protection shield buffers the shock and the ceramic ring cracks without splintering. In most cases, however, the flange is punctured and the ceramic remains intact.
With a suitable fuse the device will withstand currents of up to 150 kA and the flange will puncture. An oscillogram of a 150 kA surge current pulse and the corresponding voltage across the fuse is shown in fig. 7.

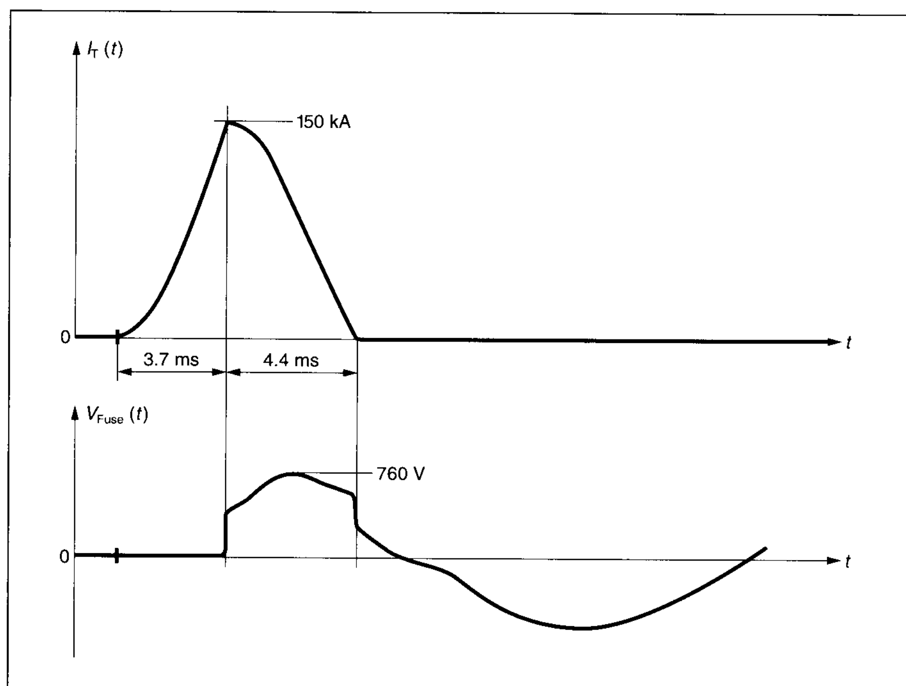

Fig. 7
Oscillogram of a short-circuit event in a fused circuit.
Upper trace: Surge current in thyristor and fuse
Lower trace: Voltage across the fuse

The higher I_{TSM} values with fuses result from the fact that the current is interrupted after 3 or 4 ms (when the i^2t limit of the fuse is reached).
In the case of non-explosion-resistant housings, the ceramic ring can crack in an uncontrolled way. This failure mode occurs above 90 kA (10 ms base, single pulse) for the N-type housing. These ratings have been confirmed in high power laboratory tests and the housing design proven to be safe below this limit through several years of field service.

5.4 PCT Design Example

The following calculation will familiarise the user with some basic PCT design rules and demonstrate the use of a PCT data sheet.

5.4.1 Assignment

- A three phase thyristor rectifier bridge is needed to control a DC motor. The line voltage is V_{Line} = 660 V (RMS), 50 Hz, and the DC current I_d = 3600 A. The thyristor is to be air cooled with a maximum ambient temperature of T_A = 40 °C.
  The surge current is expected to be I_{TSM} = 38 kA at t_p = 10 ms with V_D = V_R = 0 V. The total commutation inductance is L = 100 μH.
- A suitable PCT from ABB Semiconductors will be selected. Also, the RC circuit and a commercially available heat sink for double-sided cooling will be designed and evaluated.

5.4.2 Voltage Design

Peak amplitude of nominal line voltage:

$$V_0\,(\max) = V_{Line} \cdot \sqrt{2} = 660\,V \cdot \sqrt{2} = 933\,V$$

Voltage rating of PCT with total overshoot factor of 2.5:

$$V_{DSM} \geqslant 933\,V \cdot 2.5 = 2333\,V \longrightarrow \underline{V_{DSM} = V_{RSM} = 2600\,V} \text{ is selected.}$$

5.4.3 Device Selection

We must now select the best suited device among all 2600 V PCTs from ABB Semiconductors. These mainly differ in size and current ratings. A first approach is to check the maximum allowed case temperature for the devices under consideration. This is done according to fig. 5 of the data sheet (T_C vs. I_{TAV}); since this is an approximation, no switching losses are considered at this stage.

In a six-pulse three-phase rectifier bridge, each thyristor carries ⅓ of the DC current; the conduction angle is 120° (rectangular pulses). The average on-state current is therefore:

$$I_{TAV} = \frac{1}{3}\,I_d = \frac{1}{3}\,3600\,A = 1200\,A$$

At this average on-state current, the thyristors under consideration require the following max. case temperatures (for a max. junction temperature of 125 °C) and yield the following surge currents:

Part Number	Contact ∅	T_C (max) @ 120° rect.	I_{TSM} @ t_p = 10 ms
5STP 06D2600	34 mm	⩽ 70 °C	8 kA
5STP 16F2600	47 mm	80 °C	18 kA
5STP 24L2600	78 mm	99 °C	43 kA
5STP 33L2600	78 mm	110 °C	60 kA
5STP 45N2600	100 mm	112 °C	75 kA

Obviously, the "baby" 5STP 06D2600 is too small and the "jumbo" 5STP 45N2600 too big for this application. With respect to the case temperature, the 5STP 16F2600 would require an extremely efficient and big heat sink (air cooling!); since furthermore its surge current rating is far below the requirement, this device is not suited for this application either.

We therefore have to choose now between the 5STP 24L2600 and the 5STP 33L2600.

Since both devices are able to withstand the rated surge current, the only criterion is the power loss and the required heat sink. A rough estimation of the necessary thermal resistance *heat sink-to-ambient* (R_{thHA}) will be made:

According to fig. 4 in the data sheet (P_T vs. I_{TAV}), P_T and R_{thHA} for the two PCTs under consideration are:

- 5STP 24L2600: $P_T = 1950\,W$, $R_{thHA} \leqslant 25\,K/kW$
- 5STP 33L2600: $P_T = 1650\,W$, $R_{thHA} \leqslant 39\,K/kW$

Calculation for 5STP 24L2600:

$\Delta T_{CH} = P_T \cdot R_{thCH} = 1950\,W \cdot 5\,K/kW = 9.8\,K \approx 10\,K$; therefore

$$R_{thHA} = \frac{T_C\,(max) - \Delta T_{CH} - T_A}{P_T} = \frac{(99 - 10 - 40)\,°C}{1950\,W} \approx 25\,K/kW$$

Conclusion: A heat sink with $R_{thHA} \leqslant 25\,K/kW$ is hard to find; therefore, we choose the **5STP 33L2600** as best suited device for this application.

5.4.4 Power Loss Calculation

A more precise power loss calculation must now be performed in which switching losses are included.

On-state power losses P_T

There are basically two ways to calculate P_T:

1) $P_T = \frac{1}{3} I_d \cdot V_T\,(I_d)$:

1.1) $V_{T11} = V_{T0} + r_T \cdot I_T$:
$V_{T11} = 0.95\,V + 0.100\,m\Omega \cdot 3600\,A = 1.31\,V$;

$$P_{T11} = \frac{1}{3} 3600\,A \cdot 1.31\,V = 1572\,W$$

1.2) V_{T12} from fig. 2 (data sheet), max. curve at 125 °C:
$V_{T12}\,(3600\,A) = 1.30\,V$;

$$P_{T12} = \frac{1}{3} 3600\,A \cdot 1.30\,V = 1560\,W$$

2) P_T from fig. 4 (data sheet), 120° rect.: $P_{T2}\,(1200\,A) = 1650\,W$

Ideally, one should obtain the same result but the differences are small and due to uncertainties in reading the values from the graphs.
For the further calculations, we take $P_T = 1650\,W$.

Turn-on power losses P_{on}

The turn-on energy W_{on} is taken from fig. 16 of the data sheet.
The di/dt for commutation is:

$$di/dt = \frac{V_C}{L},$$

with V_C = commutation voltage and L = commutation inductance. V_C varies with the firing angle; the worst case arises when the commutation takes place at the maximum of the line-to-line voltage of the lines between which commutation takes place. In this case:

$V_C = V_{Line} \cdot \sqrt{2}$, therefore

$$di/dt = \frac{V_{Line} \cdot \sqrt{2}}{L} = \frac{660\,V \cdot \sqrt{2}}{100\,\mu H} = 9.3\,A/\mu s \approx 10\,A/\mu s$$

With $I_T = 3600\,A$, we obtain from fig. 16

$W_{on} = 0.2\,Ws$ and $\underline{P_{on}} = 50\,Hz \cdot 0.2\,Ws = \underline{10\,W}$.

Obviously, compared to the on-state losses, the turn-on losses are so small that they may be neglected.

Turn-off power losses P_{off}

The turn-off energy W_{off} is taken from fig. 18 of the data sheet.
The di/dt for commutation is 10 A/µs, and V_0 (worst case) is the peak value of the line voltage, i.e. V_0 (max) = 933 V. This yields

W_{off} = 3 Ws and P_{off} = 50 Hz · 3 Ws = 150 W.

As can be seen, the turn-off losses in this case are about 9% of the on-state losses.
The total power losses are

$P_{Ttot} = P_T + P_{on} + P_{off} = 1650\,W + 10\,W + 150\,W = 1810\,W.$

5.4.5 Designing the Heat Sink

The heat sink is designed for double-sided cooling. The maximum case temperature was estimated earlier in this section according to fig. 5 of the data sheet. With the total power losses known, we are now able to calculate T_C (max) exactly:

$$T_C\,(max) = T_{vjmax} - P_{Ttot}\,(R_{thJC} + \Delta R_{thJC(120°)})$$

$\Delta R_{thJC(120°)}$ is the additional thermal resistance resulting from the temperature ripple due to the 120° rectangular current pulses (see explanations in Section 3 of this book, "Data Sheet User's Guide"). The maximum thyristor case temperature then becomes:

$$T_C\,(max) = 125\,°C - 1810\,W\,(8\,K/kW + 1\,K/kW) = 108.7\,°C.$$

The difference to the previously found value (110 °C) results from the switching losses which contribute an additional ΔT_{JC} of 160 W · 9 K/kW = 1.4 K.
Assuming a safety margin of about 5 °C for the maximum junction temperature, we determine **T_C (max) = 104 °C** for further calculations.
The thermal resistance of the heat sink can now be calculated:

$$R_{thHA}\,(max) = \frac{T_C\,(max) - P_{Ttot} \cdot R_{thCH} - T_A}{P_{Ttot}} =$$

$$\frac{104\,°C - 1810\,W \cdot 3\,K/kW - 40\,°C}{1810\,W} = 32.4\,K/kW$$

5.4.6 Finding the Heat Sink

ABB Logistics Center in Västerås, Sweden, offers a program of air-cooled heat sinks and mounting clamps.
The aluminium heat sink type **5SAA 21V3500** has an R_{thHA} of 35 K/kW with forced air cooling (300 litres per second). This is slightly above the required value, but with an increased air flow rate (e.g. 500 l/s), the necessary cooling effect can be obtained.

5.4.7 RC Snubber Design

In Section 5.2, the design of an RC snubber circuit was explained in detail. We will refer to this section and the corresponding curves (fig. 4) for the following calculations.

The selected thyristor has a V_{DRM} of 2600 V, so we have to use the curves of fig. 4 b).
First we have to determine the reverse recovery charge Q from fig. 10 of the data sheet: At $di_T/dt = 10\,A/\mu s$, Q is 5800 µAs. $V_0 = 933\,V$ is the peak value of the line voltage.
The snubber is determined such that the overshoot ratio V_{RM}/V_0 is about 1.4 with the aim of having the snubber capacitor as small as possible. Therefore, the term $Q/C \cdot V_0$ in fig. 4 b) should be the maximum possible for the given overshoot ratio. We look for the maximum of the curve with $V_{RM}/V_0 = 1.4$ and find:

$$\frac{Q}{C \cdot V_0} = 1.4$$

(note: it is coincidental that this value is the same as the overshoot ratio).

The corresponding value on the horizontal axis is $R^2C/L = (1 \ldots 1.7)\ \Omega^2\mu F/\mu H$; this value will be used to calculate the snubber resistor later on.

With Q and V_0 being known, we can now calculate C:

$$\underline{C} = \frac{Q}{1.4 \cdot V_0} = \frac{5800\,\mu As}{1.4 \cdot 933\,V} = \underline{4.4\,\mu F}$$

Also R can now be calculated:

$$\underline{R} = \sqrt{(1 \ldots 1.7)\frac{L}{C}} = \sqrt{(1 \ldots 1.7)\frac{100\,\mu H}{4.4\,\mu F}} = \underline{4.8 \ldots 6.2\,\Omega}$$

Discussion of the Resulting Values:
C is quite high and R rather small. It is justified to select the next lower value that is commercially available for C (i.e. 3.3 µF) for the following reasons:

- Q has been taken from the max. curve. A *typical* Q value would yield a lower value for C.
- The overshoot factor of 1.4 is rather small. Typical ratios are 1.3 . . . 1.6. With a factor of 1.6 for example, C would only be 2.6 µF.
- The blocking voltage is somewhat higher than originally required (the calculation yielded 2333 V, see Section 5.4.2, "Voltage Design", but we selected the next higher value of 2600 V). This gives additional voltage margin.

We select therefore **C = 3.3 µF** and recalculate R. Since all curves in fig. 4 b) have their maximum in the x-axis range $R^2C/L = 1 \ldots 1.7$, we calculate with 1.7. This yields

$$R = \sqrt{1.7\frac{L}{C}} = \sqrt{1.7\frac{100\,\mu H}{3.3\,\mu F}} = 7.2\,\Omega.$$

We select the next higher standard value: **R = 8.2 Ω.**

5.5 Do You Need a Faster Switching Device?

All standard thyristors from ABB Semiconductors are optimised for low on-state power losses, i.e. low V_T values. This is possible because the very sensitive high temperature diffusion processes are highly controlled so that the charge-carrier lifetime of the electrons and holes is at a maximum, which means that turn-off parameters like Q and t_q are correspondingly high. For the majority of applications, this approach is optimal.
There are, nonetheless, applications for phase control thyristors for which the main focus is on dynamic turn-off parameters rather than on-state voltage. In this case, it is possible to request an *adapted standard* device from ABB Semiconductors, as described in Section 1 of this book, "Product Introduction and Logistics". This very useful option of tailoring static and dynamic parameters to customer's needs is practicable thanks to the use of electron irradiation to accurately control carrier lifetime. This process step is performed at the end of wafer manufacturing.

The following example illustrates the benefits of this unique service.
In the table below, three possible parameter combinations are shown for the *5STP 25L5200* phase control thyristor. There is no difference in the blocking capability between the three products, i.e. the blocking voltage of $V_{DSM} = V_{RSM} = 5200\,V$ is common to all the devices.

Product status	V_T	t_q (max)	Q (typ)	I_{TSM}	I_{TAVM}
Measurement conditions	*3000 A 125 °C*	*1.5 A/µs 20 V/µs 125 °C*	*1.5 A/µs 125 °C*	$T_C = 125\,°C$ $T_{vj} = 125\,°C$ $t_p = 10\,ms$	$T_C = 70\,°C$ $T_{vj} = 125\,°C$ *Half sine wave*
Standard	1.7 V	700 µs	3500 µAs	42 kA	2550 A
Adapted std. 1	1.9 V	400 µs	2500 µAs	38 kA	2350 A
Adapted std. 2	2.1 V	300 µs	2000 µAs	35 kA	2200 A

Designers who see advantages in such customised trade-offs are invited to contact their ABB Semiconductors' representative for further information.

5.6 Cosmic Ray Withstand Capability

As mentioned in Section 2, "Product Design", the incidence of cosmic particles on high power silicon devices can provoke spontaneous failure in the presence of high blocking voltages. This probability is commonly expressed as a failure rate (average number of failures per unit time and per device). The failure rate is measured in FITs (*f*ailures *i*n *t*ime): 1 FIT is defined as 1 failure per 10^9 hours of operation under the rated conditions. Fig. 8 depicts the failure rate as a function of applied DC voltage for ABB Semiconductors' phase control thyristors.
The failure rate is independent of the carrier lifetime; it is therefore also valid for a corresponding adapted standard product.

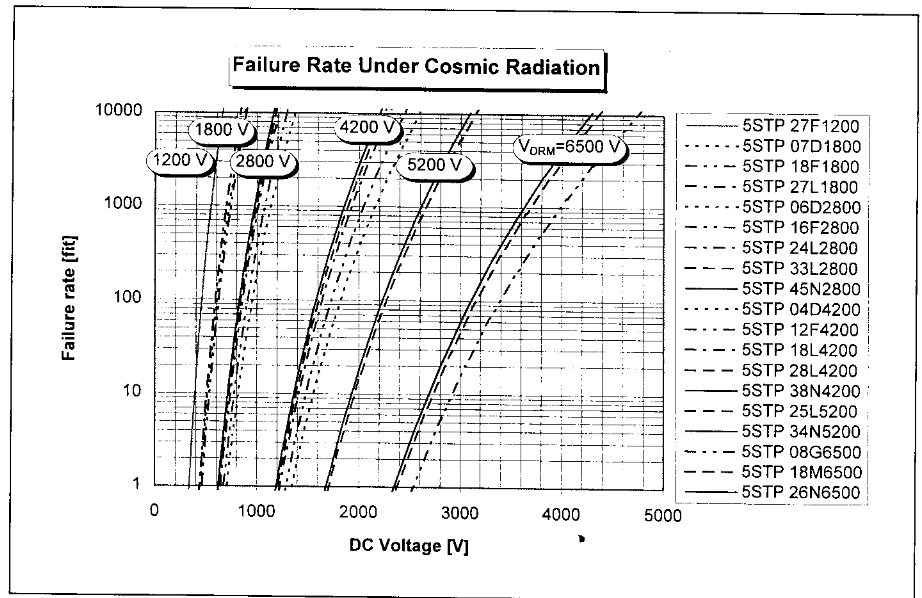

Fig. 8
Failure rate in FIT for ABB Semiconductors' PCTs. Each group of curves describes a specific voltage rating, and the difference between the devices within one voltage class results mostly from different device areas.

As an example, a 5STP 25L5200 might be used in a crowbar application at an average DC voltage of 2600 V. The thyristor would then have a failure rate of 700 FIT, which is equivalent to a mean-time-between-failures (MTBF) of $1.4 \cdot 10^6$ hours or 163 years which is, of itself, adequate. If, on the other hand, a fleet of 25 locomotives with each 4 such thyristors is circulating, an MTBF (for any locomotive to fail) would be 1/100 of 163 years or 1.6 years. In applications with varying voltages the time dependence of the applied voltage must be taken into consideration: for a chopped DC with 50% duty cycle, the failure rate would be half of the value in fig. 8. In most PCT applications, however, the devices are exposed to AC voltages well below V_{DRM} (V_{RRM}) for which cosmic radiation failure rates are negligible.