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Switching-Self-Clamping-Mode “SSCM”, a breakthrough in SOA performance for high voltage IGBTs and Diodes

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Abstract

In this paper, we present a new high voltage IGBT and diode design platform exhibiting the highest SOA limits achieved to date. We demonstrate for the first time, low loss IGBT and diode chip-sets with voltage ratings ranging from 3.3kV to 6.5kV capable of withstanding both dynamic avalanche and what we refer to as the Switching-Self-Clamping-Mode; hence, resulting in a clear breakthrough in SOA capability for high voltage devices.

Introduction

One of the main challenges today in the design of High Voltage IGBTs and diodes is the **Safe Operating Area** “SOA” capability (1). A destruction point characterises the SOA limits whereas failures are largely related to the device design and/or process. In recent years, the SOA performance for medium to low voltage devices has improved immensely. Optimised emitter cell designs, the introduction of the NPT and SPT vertical design concepts and better-controlled lifetime reduction techniques have all helped in this direction. However, previous experience and literature has clearly pointed out that the SOA performance for higher voltage devices rated above 2000V degrades significantly when compared to the low to medium voltage class devices (2)(3). This downtrend is due to physical constraints in high voltage structures and the high stress operating conditions. Furthermore, the trade-off between the optimisation of the overall losses and the SOA capability has imposed further restrictions in the design window of high voltage IGBTs.

Trends for the development of IGBTs and diodes aimed for wide SOA limits are fuelled by many requirements in applications operating under hard-switching conditions. Improved SOA performance will have a positive impact on manufacturability, reliability, power handling capability, ease of paralleling, better controllability, better system and gate drive designs aimed at reducing the total system losses, and employing more optimised protection schemes. In order to ensure that high voltage devices do not exceed their SOA limits, many restrictions were introduced for operating such devices. Therefore, system designers have resorted into setting many circuit and gate drive parameters accordingly. Such modifications include an increase in gate resistance and the inclusion of protective active clamps or snubbers. This added complexity has had normally a negative impact on the performance, cost and size of high power electronic systems.

We have continued to follow the development trend by demonstrating for the first time a high voltage IGBT and diode design platform capable of self-clamping (4) during device turn-off even when tested under extreme conditions. Therefore, enabling us to extend the device SOA capability and setting new standards for high voltage devices as shown

in Fig.1. In addition to achieving a record breaking SOA capability, the newly developed devices exhibit low losses and excellent overall electrical properties. In this paper, we outline some design and operational aspects of the new high voltage chips plus the latest results obtained for 3.3kV, 4.5kV and 6.5kV devices.

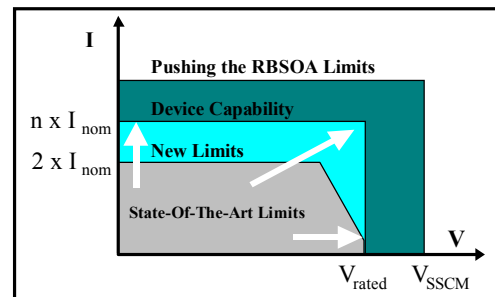


Fig. 1: Extending the RBSOA limits of HV-IGBTs And Diodes.

Switching-Self-Clamping-Mode in HV Devices

Dynamic cell latch-up represents the main failure mode when the IGBT turns off especially under extreme dynamic avalanche conditions. These conditions include high current, high voltage, high temperature, large inductance and low gate resistance values. Failures normally occur when the IGBT N+ source injects enough electrons into the P channel region to cause uncontrolled parasitic thyristor triggering leading to device failure. Protection of the N+ source region is vital for increasing the cell latch-up immunity of IGBTs.

Diodes are also limited in their SOA due to dynamic avalanche during reverse recovery. Under the adverse combination of high commutating di/dt, high current densities and high temperatures, the diode is forced during reverse recovery into dynamic avalanche. Extra carriers are then generated that are sensitive to any non-uniformities in the device structure leading to destructive current filaments forming in the device. Optimisation of the diode termination design, process and lifetime control has reduced the risk of filaments occurring during dynamic avalanche resulting in stable reverse recovery performance (5).

However, for high voltage devices with typical low background doping concentrations, the removal of the electron-hole plasma during device turn-off forces the device into a strong dynamic avalanche mode at much lower currents when compared to lower voltage devices. Therefore, limiting substantially the SOA performance of high voltage IGBTs and diodes. We will show in this paper that all typical dynamic avalanche failure modes caused by the removal of the electron-hole plasma can be eliminated. Thereafter, this has led to the device experiencing a self-clamp avalanche

mode during turn-off similar to that obtained in a standard unclamped inductive test. We refer to this as the **Switching Self-Clamping Mode (SSCM)**, where the device overshoot voltage reaches a value V_{SSCM} close to the static breakdown voltage of the device as shown in Fig.2.

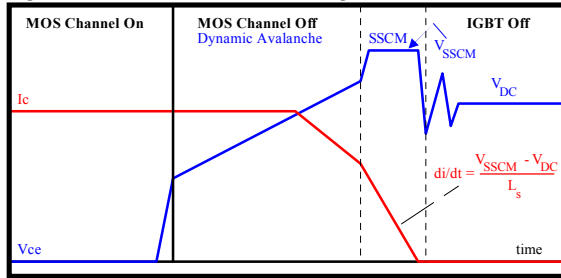


Fig. 2: IGBT SOA turn-off waveforms including SSCM

As the voltage rises, the IGBT goes into dynamic avalanche immediately after the MOS channel ceases to inject electrons into the n-base region. The lack of electron compensation for the recovering holes will modify the effective background doping and electric field distribution characterised by the lower dv/dt value during dynamic avalanche. Unless device failure occurs, the dynamic avalanche phase continues until the remaining electron-hole plasma is used up and subsequently dynamic avalanche is suddenly eliminated. Because of the stray inductance in the commutation circuit, the voltage over the IGBT starts to rise and eventually reaches the breakdown voltage of the pn-junction, whereas avalanche-generated carriers will carry the reverse current in the IGBT. Optimum design of the device buffer region by employing a Soft-Punch-Through SPT concept will enable the device to withstand such conditions by self-clamping the overshoot voltage successfully. Thus, leading to an ultimate square SOA capability up to the device blocking voltage.

New High Voltage IGBT and Diode Design Platform

In order to achieve excellent static and dynamic characteristics for the IGBT and diode, the latest IGBT and diode technologies employ the Soft-Punch-Through concept shown in Fig.3. This approach has helped us to take a considerable leap in reducing the over-all losses of the device when compared to older designs (6).

The addition of a low doped and deep SPT buffer region realises a reduction of 20% of the total device thickness when compared to an NPT design. However, this approach demands a higher resistivity starting material with lower punch-through voltages to achieve the required blocking voltage combined with low cosmic ray failure rates. The SPT buffer then ensures that such a device maintains soft turn-off characteristics. In addition to these advantages, we demonstrate here that by further optimisation of the SPT design, major benefits will result in improving the SOA performance of both the IGBT and diode.

A. New HV-IGBT design platform: In addition to the SPT buffer region, different anode concepts were investigated and tailored for the required on-state and turn-off losses. The optimisation of the SPT buffer and anode design had also a major impact on increasing the short circuit capability for the new HV-IGBT range as discussed later in the article.

Furthermore, the new HV-IGBT design platform utilises an advanced and extremely rugged planar stripe cell design. The new technology was developed mainly for increasing substantially the cell latch-up immunity for a wide SOA performance. The main approach was to carefully optimise the IGBT cell pn junction profile while on the other hand, increase the protection level of the N+ source region especially at the weakest point near the MOS channel. Standard cell optimisation steps for determining the cell spacing and cell opening were undertaken for providing strong plasma enhancement at the emitter side. A scaling factor was also established for scaling up the cell design platform for all the voltage range. The scaling parameters include the cell opening and cell spacing while maintaining a constant area ratio of both parameters. This scaling approach ensures an optimum low loss design and achieves good switching and short circuit performance even for devices rated up to 6.5kV.

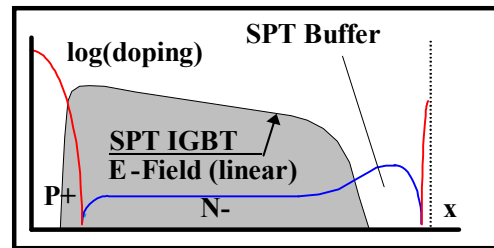


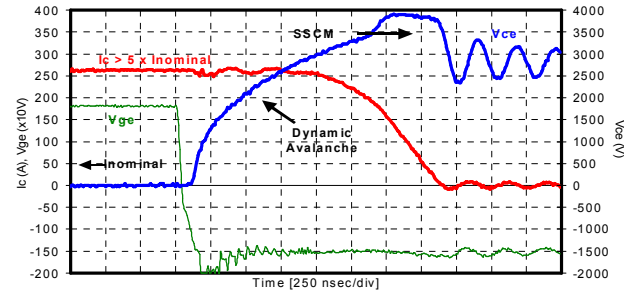
Fig. 3: SPT IGBT doping profile and field distribution

B. New HV-diode design platform: The superior SOA performance of the new HV-diodes was reached by applying the following design features. Firstly, a higher doped P+ anode was employed; thus, resulting in an extremely rugged performance when compared to lower P anode diodes. This is due to a reach-through effect during reverse recovery when the device is tested under extreme dynamic avalanche conditions. At high current densities, the holes generated at the pn junction during dynamic avalanche will compensate for the acceptor ions of low-doped P anode profiles. Therefore at a given current level, the field slope will decrease, resulting in the electric field reaching the anode contact and subsequently leading to a device failure. The higher P+ doped anode has also aided in developing a robust junction termination design to eliminate any possible drawbacks in terms of device ruggedness due to high fields and current crowding at the anode periphery during reverse recovery. Finally, using a combination of local and homogenous lifetime control methods, the electron-hole plasma can be shaped in an optimal way for tailoring the electrical parameters and improve the SOA performance.

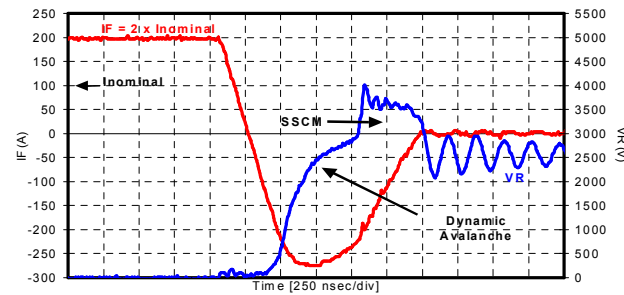
New High Voltage IGBT and Diode Performance

The new 3.3kV IGBT and diode set a new standard in terms of turn-off RBSOA performance. This can be clearly seen in the RBSOA waveforms shown in Fig.4a and Fig.4b for the 3.3kV/50A IGBT and 3.3kV/100A diode respectively when operating under extreme conditions with no active clamps or snubbers employed in the test set-up. The oscillations observed in the current and voltage waveforms are a consequence of the high overshoot voltage, high stray inductance and low device output capacitance during SSCM.

Under normal operating conditions, the chip-set exhibits low losses, soft switching waveforms and excellent overall electrical properties as shown in Fig.5.

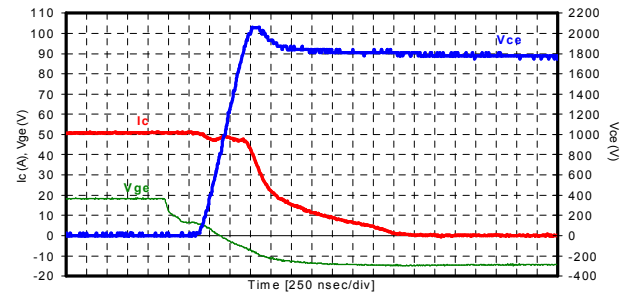


(a) IGBT Turn-off RBSOA waveforms
 $V_{DC}=2700V, I_c=260A$
 $V_{SSCM} > 3800V, P_{peak} = 0.75MW/cm^2$

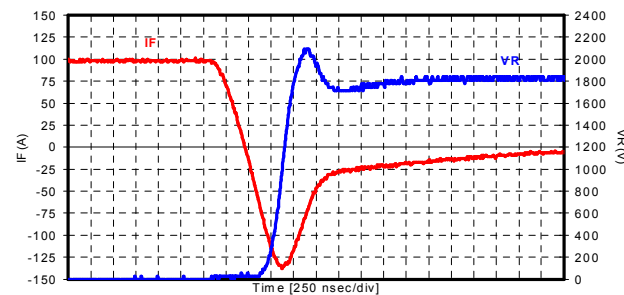


(b) Diode Reverse Recovery RBSOA waveforms
 $V_{DC}=2500V, I_F=200A, di/dt=1000A/\mu sec$
 $V_{SSCM} > 3500V, P_{peak} = 0.8MW/cm^2$

Fig. 4: 3.3kV/50A IGBT and 3.3kV/100A diode RBSOA switching characteristics @125°C, $R_G=0\Omega, L_S=2.4\mu H$



(a) IGBT Turn-off waveforms at $I_c=50A$



(b) Diode Reverse Recovery waveforms at $I_F=100A$

Fig. 5: 3.3kV/50A IGBT and 3.3kV/100A diode nominal switching characteristics @125°C, $V_{DC}=1800V, R_G=33\Omega, L_S=2.4\mu H$

Typical nominal condition losses are outlined in table (1) along with the new 4.5kV and 6.5kV IGBTs. All devices exhibit a positive temperature coefficient at rated currents. To demonstrate a similar RBSOA performance for higher

voltage class IGBTs with the same design platform, Fig.6 and Fig.7 show RBSOA turn-off waveforms for a 4.5kV/40A IGBT and two paralleled 6.5kV/25A IGBTs respectively. We must point out that the devices were tested under extremely high stray inductance values.

TABLE 1 Typical Losses	Current Density A/cm ²	V _{ce} Volt 25°C	V _{ce} Volt 125°C	E _{off} /V _{dc} mJ/Volt 125°C
3300V Diode	100	2.3	2.35	-
3300V IGBT	50	3.1	3.8	80/1800
4500V IGBT	40	3.3	4.4	170/2800
6500V IGBT	30	3.6	4.7	180/3600

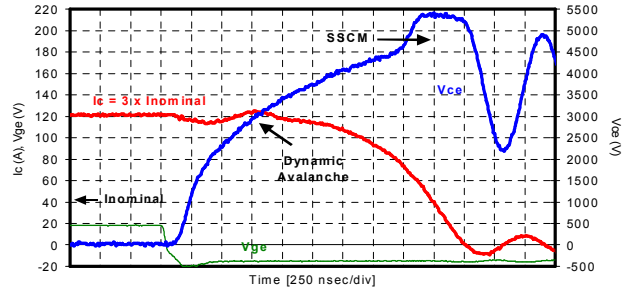


Fig. 6: 4.5kV/40A IGBT Turn-off RBSOA waveforms
 $V_{DC}=3600V, I_c=120A, 125^\circ C, R_G=0\Omega, L_S=12\mu H$
 $V_{SSCM} > 5300V, P_{peak} = 0.5MW/cm^2$

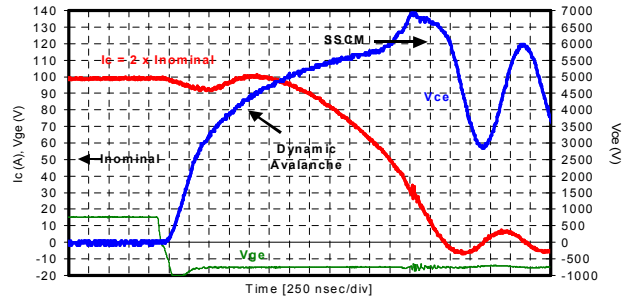


Fig. 7: 6.5kV/2x25A IGBT Turn-off RBSOA waveforms
 $V_{DC}=4500V, I_c=100A, 125^\circ C, R_G=0\Omega, L_S=20\mu H$
 $V_{SSCM} > 6500V, P_{peak} = 0.25MW/cm^2$

It is necessary to point out here that one of the many advantages of an extremely rugged IGBT is the possibility of operating the device with lower gate resistance R_G values. Thus, resulting in much lower losses and shorter delay times during device turn-off. We have clearly observed that long delay times can result in large current redistributions between parallel IGBTs and hence a significant loss in SOA capability. The conventional technology would require a significantly higher gate resistance value to achieve the required turn-off current capability when compared to the new technology. As seen in Fig.8, while for the conventional technology a significant de-rating from a single chip capability has to be accepted when chips are parallel connected, the switch-able current per silicon area is basically independent of the number of parallel-connected chips for the new technology operated with a lower R_G . It is worth pointing out that for the conventional IGBT technology, the use of even higher gate resistance values for compensating the loss

in turn-off capability will only result in a further increase in the de-rating factor and also higher turn-off losses.

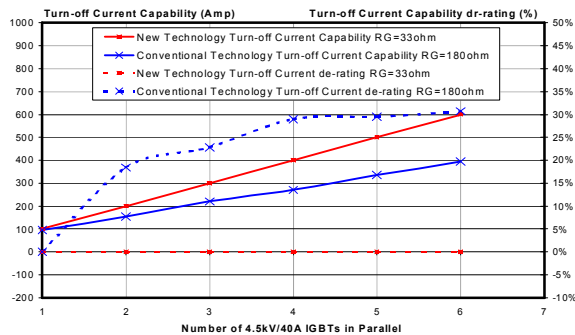


Fig. 8: Comparison of turn-off current capability in parallel-connection of conventional and the new 4500V IGBT chips

To investigate the performance of the new chip-set in parallel operation, devices were assembled in a standard 3.3kV/1200A rated module containing 24 IGBTs and 12 diodes. Fig.9 shows a remarkable IGBT RBSOA turn-off waveform from a collector current of 5000A. The IGBT can clearly demonstrate its ruggedness even under heavy paralleling during both dynamic avalanche and SSCM modes of operation.

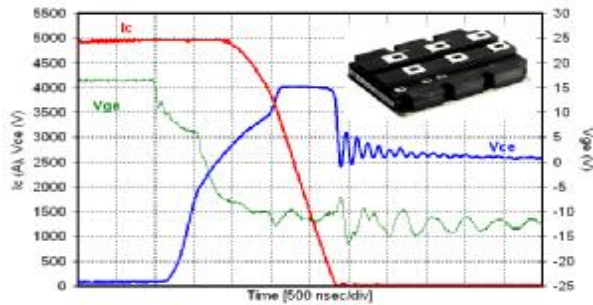


Fig. 9: 3.3kV/1200A IGBT Module Turn-off RBSOA waveforms
 $V_{DC}=2600V, I_C=5000A, 125^{\circ}C, R_G=1.5\Omega, L_S=280nH$

IGBT Short Circuit Performance

The short circuit SOA ruggedness represents a major challenge especially for high voltage punch-through type IGBTs. Short circuit current pulse failures occurs typically at a relatively well defined, design specific current density immediately after turn-on or during the short circuit pulse. We also observed that such failures occurred at low dc link voltages close to the punch-through value.

The short circuit current increases significantly at lower temperatures or as a result of gate voltage pumping during some failures experienced in the application (voltage increase during IGBT conduction leading to pumping of V_{ge} through the gate collector capacitance). For that reason, it is necessary for IGBTs to withstand short circuit conditions under gate voltages exceeding the 15V standard drive voltage.

The high levels of conducting electrons during the short circuit pulse will result in unbalanced carrier concentrations in the n-base. These carriers will modify the effective background doping and subsequently lead to large distortions in the electric field distribution. Such behaviour will give rise

to a negative differential resistance effect normally accompanied with high current filament formations that eventually can lead to the destruction of the device. Increasing the SC SOA by lowering the short circuit current of the IGBT has been the standard approach, but this is done at the expense of increased on-state losses and turn-on losses. The optimum SPT buffer and anode designs employed in the IGBT are essential for obtaining a high short circuit SOA capability. Fig.10 shows the short circuit performance for the 6.5kV/25A IGBT under a high gate emitter voltage, high current density and high dc link voltage.

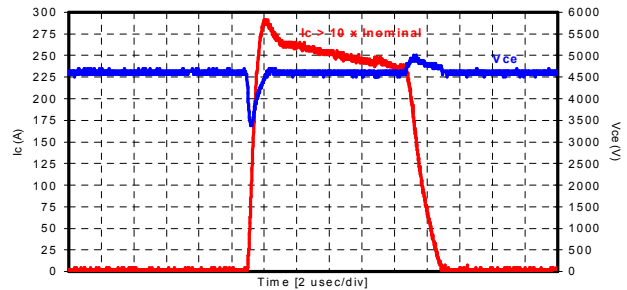


Fig. 10: 6.5kV/25A IGBT Short Circuit waveforms
 $V_{DC}=4500V, V_{ge}=18.0V, 25^{\circ}C, L_S=2.4\mu H$
 $I_{peak} = 290A, P_{peak}=1.35MW/cm^2$

Conclusion

A new high voltage IGBT and diode platform was presented. The newly developed technology concepts have resulted in a clear breakthrough in SOA performance especially for higher voltage devices rated up to 6.5kV. Both IGBTs and diodes were designed to exhibit very wide SOA limits even under extreme test conditions, while still maintaining lower conduction and switching losses when compared to older generation devices. The presented new benchmark in SOA performance will provide a new outlook for system designers, enabling a far more optimum performance of high voltage power electronics applications.

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