A Study of Switching-Self-Clamping-Mode "SSCM" as an Over-voltage Protection Feature in High Voltage IGBTs

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Abstract

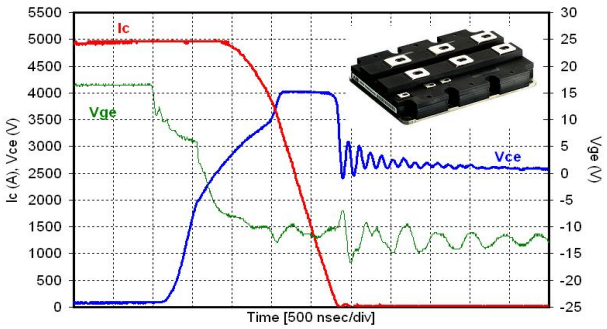
In this paper, we study the Switching-Self-Clamping-Mode "SSCM" in high voltage IGBTs in terms of device physics and circuit operation. We present analysis for the HV-IGBT failure mode when operating in SSCM due to an unstable negatively damped system and the design consideration taken into account for avoiding such mode of operation. This will enable the introduction of an over-voltage protection feature during device turn-off to add to the existing over-current protection capability under short circuit conditions.

Introduction

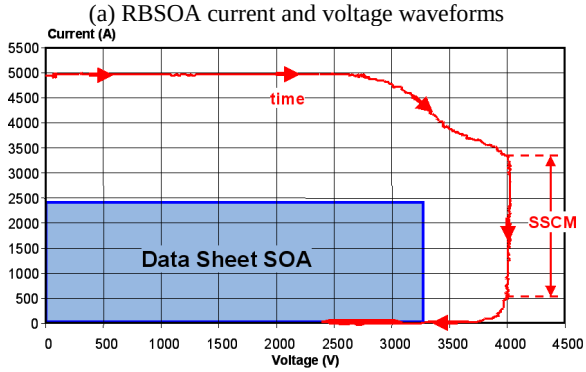
Trends for the development of IGBTs have always aimed to obtain a sufficiently large safe operating area (SOA) as required by many power electronic systems operating under hard-switching conditions. The IGBT has an inherent short circuit withstand capability, which provides an effective over-current protection level under fault conditions. However, in the case of large overshoot voltages occurring during device turn-off, state-of-the-art high-voltage IGBTs do not yet have a protection method due to the limited RBSOA capability when compared to low voltage IGBTs [1]. To overcome the insufficient IGBT ruggedness, device manufacturers and system designers in the past resigned themselves to a number of operational limits such as de-rating and the use of voltage clamps, snubbers and high gate resistances, to achieve the necessary switching capability.

A new high voltage SPT-IGBT design platform with extremely high SOA capability has been presented [2]. This new technology enables the devices to withstand the critical, formerly unsustainable, phase of dynamic avalanche resulting in a remarkable increase of ruggedness. The new generation of IGBTs is able to reach a new operational mode, which we refer to as the Switching Self-Clamping Mode (SSCM), characterised when the overshoot voltage reaches levels close to that of the static breakdown voltage. We demonstrated that the IGBT could still remarkably withstand such conditions leading to an ultimate square SOA behaviour. This mode of operation can be seen in the 3.3kV/1200A IGBT module RBSOA waveforms shown in figure (1:a) and the associated square SOA I/V curve in figure (1:b).

In this paper, we propose that the new SSCM capability can be utilised effectively as an added protection feature to bring IGBTs to a remarkable level of safe operation with a total package for **over-voltage and over-current protection** mechanisms included solely in the IGBT structure.



(a) RBSOA current and voltage waveforms



(b) I/V square RBSOA curve

Fig. 1: 3.3kV/1200A IGBT module RBSOA at 125°C
V_{DC}=2600V, I_C=5000A, R_G=1.5Ω, L_S=280nH
Energy =20J, P_{peak} = 14MW, V_{SSCM} = 4000V

To give a better understanding of the device behaviour under dynamic avalanche and SSCM conditions, we present a detailed physical analysis of the IGBT when operating under SSCM and the failure mechanisms associated. We have concluded that the cause of failure once an IGBT enters the SSCM mode of operation is due to the system entering an **unstable negatively damped mode** of operation. We explain the IGBT failure mode along these lines and discuss the required design trends for SPT-IGBT type structures when compared to previous NPT structures [3]. We also present the IGBT parallel operation and current sharing during SSCM mode. In addition, results from repetitive tests under SSCM will be presented to demonstrate the safe use of the IGBT to carry out its self-protection task. The effects of test parameters on the device self clamp performance are included for a wide range of currents, temperatures and stray inductances. The high dynamic avalanche ruggedness, combined with safe SSCM performance gives users the greatest freedom in designing their systems without the need for any dv/dt or peak-voltage limiters such as snubbers or clamps.

SPT Design for Safe SSCM Performance

There has been extensive research into failure modes during power device turn-off [4]. The dependence of the electric field on the effective background doping of modern SPT type IGBTs structures has led to the device experiencing new failure modes during turn-off as well as during short circuit operation of the IGBT [5]. The high levels of conducting electrons due to short circuit operation or pn-junction avalanche during turn-off can result in unbalanced carrier concentrations in the n-base. These carriers will modify the effective background doping and subsequently lead to large distortions in the electric field distribution. Such behaviour will give rise to a negative differential resistance effect normally accompanied with high current filament formations that eventually can lead to the destruction of the device [6]. A good understanding of the filament formation and subsequent failure mode has required further investigations.

We have observed that the SPT-IGBT inherits a clear trade-off between three important design parameters; namely the short circuit SCSOA, SSCM withstand capability and leakage current. The optimisation of the IGBT internal PNP bipolar transistor gain β_{pnp} plays the key role in the optimisation process as shown in figure (2).

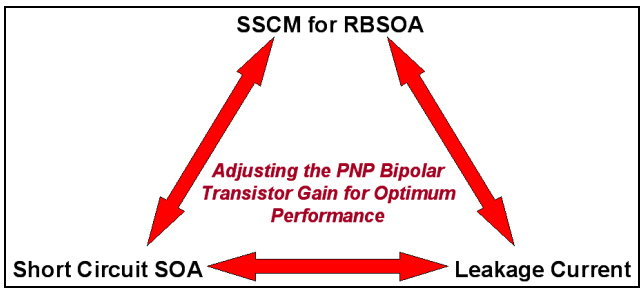


Fig. 2: The art of SPT design in high voltage IGBTs

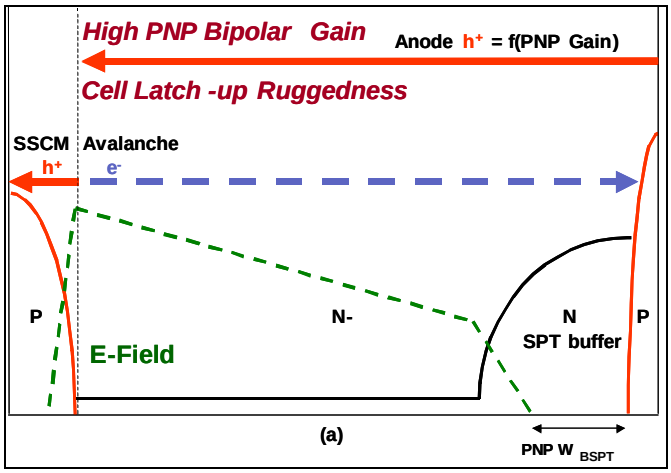
The bipolar transistor gain β_{pnp} is given by

$$b_{pnp} = \frac{D_{pSPT}}{D_{nC}} \frac{L_{nC}}{W_{BSPT}} \frac{N_{AC}}{N_{DSPT}} \left(\frac{n_{ieB}^2}{n_{ieC}^2}\right) \qquad (1)$$

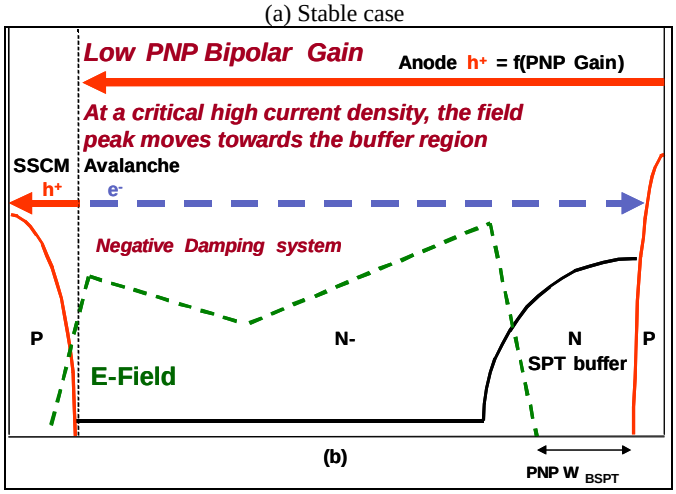
β_{pnp} is dependent on the un-depleted base width in the SPT buffer W_{BSPT} at voltages above the punch-through value. Where N_{DSPT} and N_{AC} represent the background doping of the un-depleted SPT buffer and the IGBT p-type collector or anode respectively. Also, D_{pSPT} and D_{nC} are the minority carrier diffusion coefficients in the un-depleted SPT buffer and collector respectively. Finally, L_{nC} is the diffusion length of electrons in the collector.

A narrower W_{BSPT}, lower N_{DSPT} and/or higher N_{AC} values will result in increased gain levels. The investigation shows that a high gain design will always improve the SCSOA and SSCM capability while having the drawback of increased leakage currents. The SPT-IGBT SSCM and Short Circuit withstand capability can be adjusted through the optimum choice of parameters for the PNP Transistor Gain in the IGBT while keeping low levels of leakage current.

In case of a non-optimised low gain design, the cause of failure is due to the IGBT forcing the system into an unstable negatively damped mode of operation [7] as shown in figure (3:a & 3:b) for a stable and unstable SSCM case respectively. The unstable mode is triggered at a critical current density during SSCM and SCSOA for given design parameters, and subsequently due to a low gain value, the compensation of electrons is not sufficient to maintain a normal electric field distribution resulting in a peak field near the SPT buffer. Therefore, the IGBT design must ensure that the system's damping ratio remains positive for withstanding SSCM and SCSOA operation.



(a) Stable case



(b) Unstable case

Fig. 3: SPT-IGBT structure during SSCM

Characterisation of SSCM for a 3300V IGBT Module

In order to gain a better understanding and to determine the effective and reliable operation of IGBTs in SSCM, extensive testing was carried out for the 3300V IGBTs under a wide range of operating conditions. We clearly demonstrated the feasibility of parallel operation of high voltage IGBTs chips under extreme dynamic avalanche and SSCM conditions as shown in the module results presented previously. A number of tests were carried out in order to take a closer look at the current sharing between paralleled IGBTs under such SOA conditions, no clamps or snubbers we used in these tests.

A 3300V/1200A module with 3 separate legs in parallel was tested at 4000A and 2.65kV DC link voltage. The current was recorded for each leg as shown in figure (4). The waveforms show very uniform current sharing between the 3 legs even as

the module enters the dynamic avalanche and SSCM stages of operation.

A percentage of deviation of around 1% was observed between the current in each leg of the module. This represents a negligible value, and therefore there are no contributions into the current de-rating of the module due to parallel mismatch under SOA conditions. It is important to point out that the use of lower gate resistance values (R_{Goff}) than those required by conventional technologies results in shorter delay times during device turn-off. Hence, improving the current sharing between individual IGBT chips in the module.

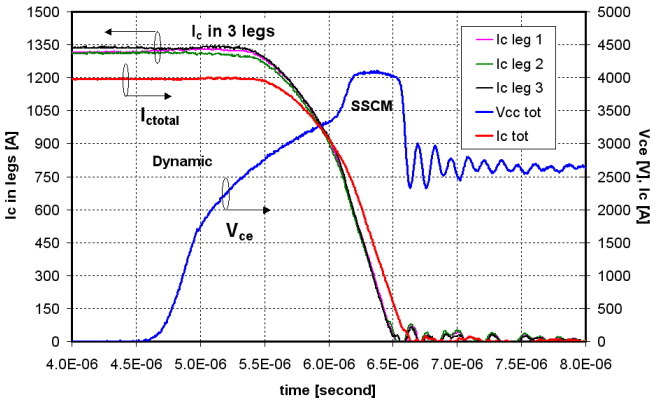
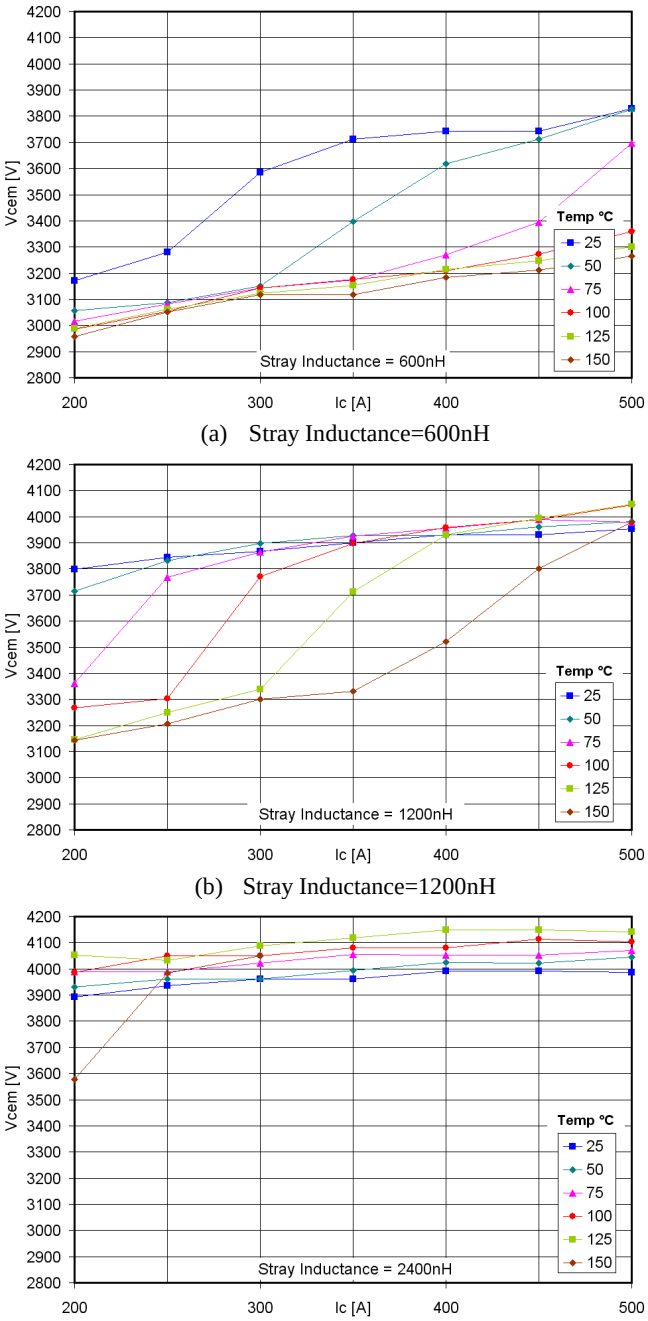


Fig. 4: 3.3kV/1200A IGBT module RBSOA at 125°C
V_{DC}=2650V, I_C=4000A, R_G=1.5Ω, L_S=280nH

To investigate the stability of the IGBT turn-off performance under a wide range of operating conditions, 3300V/200A IGBT substrates consisting of 4 IGBTs were tested with a DC link voltage of 2650V at different temperatures, currents and stray inductance values. Figure (5) shows the relationship between the maximum voltage V_{cem} and collector current I_c for temperatures ranging from 25°C up to 150°C. The tests were carried out for 3 values of stray inductance; 600nH, 1200nH and 2400nH. This is equivalent to module stray inductance values of 100nH, 200nH and 400nH respectively.

The trends show that the IGBT maximum overshoot voltage is highly dependent on the three parameters under observation. At a low stray inductance value of 600nH, the device does not enter into SSCM mode (~4000V) for temperatures higher than 50°C and up to 500A, which represents 2.5 times the rated current of the substrate. However, at 1200nH, a clear trend is observed for the whole range of temperatures. Here we can clearly observe the relationship between the temperature and current value at which the device starts to enter into SSCM.

By doubling the stray inductance value to 2400nH, all measurements show the IGBT in SSCM even at rated current. The test at 150°C and 350A resulted in a device avalanche failure due to the combination of high temperature and SSCM, indicating the device limits of operation under these extreme conditions.



(a) Stray Inductance=600nH

(b) Stray Inductance=1200nH

(c) Stray Inductance=2400nH

Fig. 5: I_c vs. V_{cem} for 3.3kV/200A IGBT substrate Test
V_{DC}=2650V, R_G=8.2Ω

The results show the following dependencies:

1. A strictly positive temperature coefficient of the collector-emitter voltage V_{ce} is found during SSCM, which is essential for stable current sharing during this operational mode.
2. A strictly negative temperature coefficient of V_{ce} is found during dynamic avalanche condition prior to SSCM, which indicates possible thermal limitations regarding the current sharing during dynamic avalanche.

Figure (6) shows the RBSOA turn-off waveforms at 25°C and 125°C. However, despite the negative temperature coefficient during dynamic avalanche, the device remains in a safe switching mode due to the positive coefficient of V_{ce} as a function of the collector current as shown in figure (7) at

150°C, which is essential for good current sharing among paralleled IGBTs.

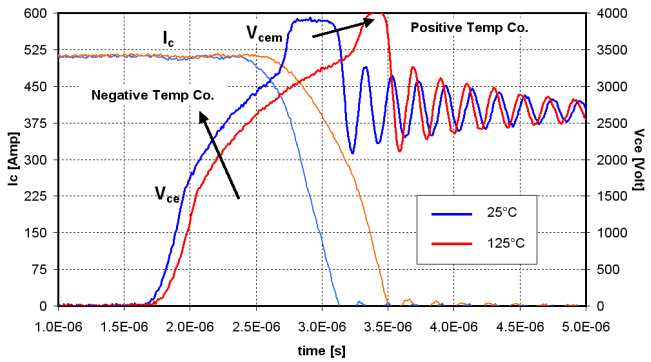


Fig. 6: 3.3kV/200A IGBT substrate RBSOA at 25°C and 125°C
V_{DC}=2650V, I_C=500A, R_G=8.2Ω, L_S=1200nH

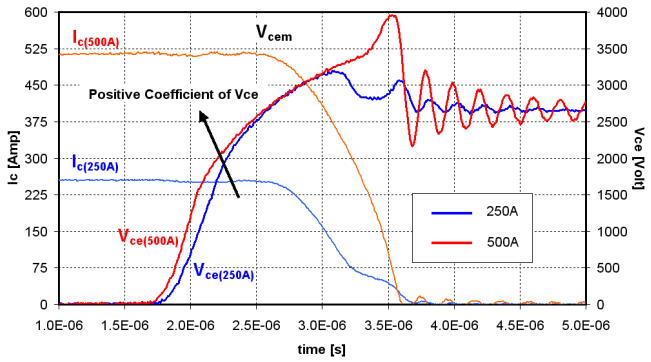


Fig. 7: 3.3kV/200A IGBT substrate RBSOA at 150°C
V_{DC}=2650V, I_C=250A and 500A, R_G=8.2Ω, L_S=1200nH

Finally, a repetitive test of a 1200A/3300V IGBT module was carried out at 125°C. The module was subjected to a defined sequence of **100 turn-off pulses** with a repetitive rate of **20 seconds/pulse** to eliminate any device heating effects after each pulse. Figure (8) shows the turn-off waveform of the IGBT under extreme dynamic avalanche conditions and SSCM using a stray inductance value of 170nH. The module was tested at 4 times rated current and 2.65kV DC link voltage. The device passed this repetitive test showing no signs of degradation after the test. This means that the module is capable of withstanding such extreme conditions for utilisation in self-protection purposes in the application.

All the results obtained point to the direction of extremely stable operation under all operating conditions within the limits of device capability. These results will help system designers to optimise their circuit parameters in order to make use of the new over-voltage protection feature when voltage overshoots occur or under any faulty operating events which normally require voltage limiters.

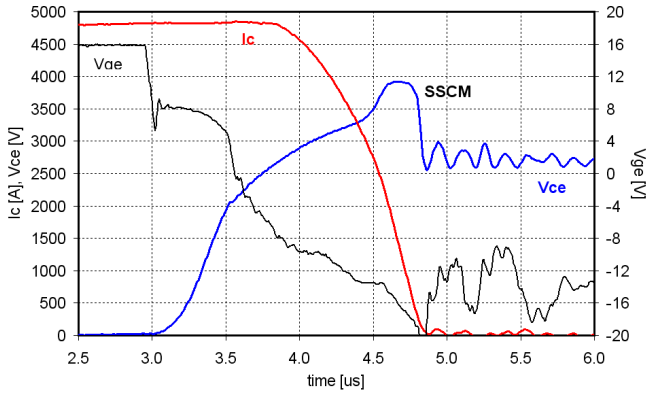


Fig. 8: 3.3kV/1200A module turn-off in repetitive mode at 125°C.
V_{DC}=2650V, I_C=4800A, R_G=1.5Ω, L_S=170nH, **100 pulses**

Conclusion

We presented a study of the Switching-Self-Clamping-Mode "SSCM" in high voltage SPT-IGBTs in terms of device physics and circuit operation. We have shown the safe SSCM operation can be realised through design consideration of the IGBT SPT structure. The overcompensation of electron represents the main theme for avoiding a negatively damped system and for the device SSCM capability. We have also presented SSCM characterisation results for a 3.3kV IGBT module for utilising the SSCM safe mode as an over-voltage protection feature during device turn-off. The presented new protection feature included in the IGBT structure will provide a completely new outlook for system designers enabling a far more optimum performance of high voltage applications.

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