

Novel Enhanced-Planar IGBT Technology Rated up to 6.5kV for Lower Losses and Higher SOA Capability

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Novel Enhanced-Planar IGBT Technology Rated up to 6.5kV for Lower Losses and Higher SOA Capability

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Abstract - In this paper, we introduce an IGBT planar technology, which sets a new performance benchmark in terms of losses and SOA capability. The improved trade-off relationship between on-state losses $V_{ce(sat)}$ and turn-off losses E_{off} (i.e. technology curve) was solely realized by means of planar cell enhancement. Simultaneously, high levels of turn-off ruggedness (RBSOA) were obtained with the new cell design. The Enhanced-Planar IGBT technology is implemented on the Soft-Punch-Through (SPT) buffer concept for ensuring controllable and soft switching behaviour. The paper will cover design details of the Enhanced-Planar technology and a full set of results for the 6500V EP-IGBT chip.

I. INTRODUCTION

Until recently, the trench concept was considered the only possibility to obtain a significantly improved performance with respect to currently available IGBTs. In this paper, we demonstrate that a high performance IGBT with ultra-low losses can be achieved using an Enhanced-Planar “EP-IGBT” technology combined with the SPT concept. Figure 1 shows two curves comparing the new enhanced planar technology with the standard design obtained from fabricated IGBTs with voltage ratings ranging from 1200V up to 6500V. The values for $V_{ce(sat)}$ were obtained at the same current density while maintaining similar turn-off losses for each given voltage class.

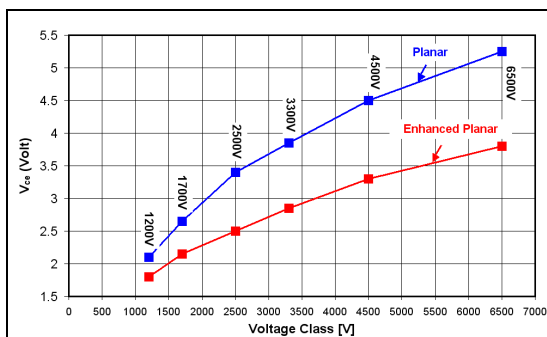


Fig. 1: Enhanced-Planar IGBT on-state losses improvements for voltage ratings up to 6500 V.

The improvement in on-state losses were achieved exclusively through enhancement of the carrier profile near the cell (emitter) while maintaining the same drift region thickness as for the standard design. The reduction in $V_{ce(sat)}$ due to cell enhancement ranges from 15% for the 1200V IGBT up to 30% for the 6500V IGBT, which is comparable to that achieved using trench technology. Against previous design trends, results show that despite the much lower on-state and switching losses, the EP-IGBT exhibits as extreme turn-off ruggedness and high levels of short-circuit withstand capability as for the standard planar design [1]. In addition, the SPT structure ensures good switching controllability and soft turn-off waveforms. In this

paper, we will examine the design of the new Enhanced-Planar IGBT cell technology and its associated performance. The key electrical characteristics of fabricated 25A/6500V prototype EP-IGBTs are presented. The devices exhibit extremely low on-state losses and high SOA limits not achieved to date for this specific voltage class. This new benchmark will provide high voltage system designers with enhanced current ratings and simplified cooling while maintaining the newly acquired robustness of high voltage IGBTs.

II. CARRIER ENHANCEMENT IN THE IGBT

For a given IGBT technology curve, optimizing for lower on-state losses by adjusting the carrier concentration near the buffer/anode region will increase the turn-off losses, which is restricted by the targeted frequency of operation. Therefore, an improved technology curve can only be achieved either by reducing the thickness of the n-base region or by lifting the carrier concentration near the emitter. The trend for reducing the device n-base thickness for improving the losses trade-off relationship has always been accompanied by an increase in the resistivity to achieve the targeted reverse bias avalanche capability and the required cosmic ray failure rate level. Thinner IGBTs with SPT type buffer designs are fast reaching their silicon design limits. Any further optimisation for lower losses will jeopardise the usefulness of these devices in many applications with regard to SOA, leakage current, controllability and softness [2].

Increasing the carrier concentration near the cells (emitter) leads to a strong reduction of $V_{ce(sat)}$ without appreciably increasing turn-off losses. Therefore, IGBT designers in the past decade have devoted their improvement efforts in this direction. The initial trends were focused on the planar cell design through the optimization of the cell dimensions and the cell doping profiles. Nevertheless, the planar design shown in Figure 2a maintained strong dependency on the following interacting effects for limiting carrier enhancement near the emitter:

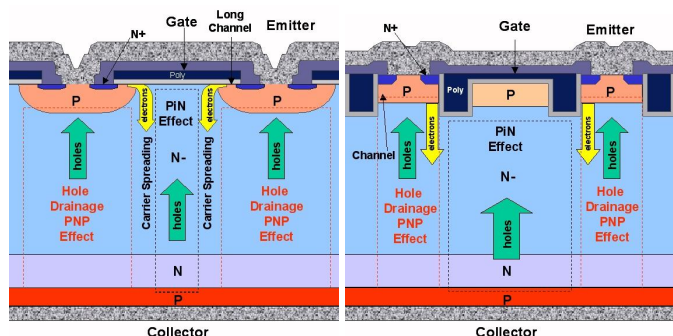
- Channel resistance; channel length & width (density)
- Carrier spreading at the MOS channel
- Carrier drainage at the cells (PNP Effect)
- Carrier accumulation between the cells (PiN Effect)

The common aim for effective carrier enhancement techniques consists of de-coupling the above effects. Therefore, lower losses were achieved by means of fine pattern and lower p-type doping concentrations in the cell for reducing the channel resistance and PNP hole drainage, and wide pitches for strengthening the PiN effect over the PNP effect [3]. In addition, a strong

trade-off between the IGBT losses and SOA (during turn-off and short circuit) continued to limit the design window for further substantial reductions in the losses. Subsequently, two methods originally employed for power MOSFETs were introduced for IGBTs, offering a better solution for improving the device losses [4];

Trench Cell Concepts: The trench design benefits from its vertical MOS channel for eliminating the current spreading effect and lowering the channel resistance by using highly packed narrow trench cells as in low voltage MOSFETs. However, the IGBT trench architecture has inherently other design requirements. The desired plasma enhancement in the PiN region, and the controlled short circuit current level, are not an outcome of using the classical approach. Therefore, wider and deeper trenches were investigated to obtain the strongest possible PiN effect. Such designs were overshadowed by practical limitations (short circuit levels remained high) and technological difficulties (etching, poly filling), which had to be overcome by making certain adjustments.

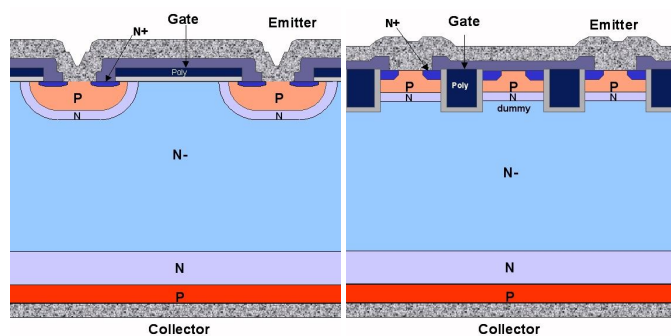
Modern trench IGBT layouts have evolved to non-repetitive narrow trench cells separated by accumulation regions, which closely resembles the wide trench effect as shown in figure (2.b). Designers have also resorted to making many cells inactive “dummy” (i.e. not contacted to the emitter, Figure 3.b) for enhancing the PiN effect while reducing the short circuit current density. However, both solutions no longer benefit from an effective electron accumulation layer adjacent to the MOS channel, which is very advantageous in terms of increasing the PiN effect. Therefore, when compared to the ideal wide and deep trench designs, a percentage of improvement in on-state losses had to be sacrificed. Nevertheless, today’s trench IGBTs maintains a clear advantage over standard planar designs in terms of lower on-state losses [5].



(a) Standard Planar (b) Non-Repetitive Narrow Trench
Fig. 2: Planar (a) and Trench (b) IGBT during conduction.

Enhancement Layer Concepts: In order to reduce the JFET effect in planar power MOSFETs, a lightly doped n-type layer (slightly higher than the n-base doping) was placed between the cells or by encompassing the cell’s p-well. However, when the n-layer extended beyond the p-well’s maximum depth, a substantial drop in the device blocking capability was observed. This method was proven to be also effective in IGBTs structures for bringing about the desired increase in the plasma density near the emitter. The higher the n-layer doping concentra-

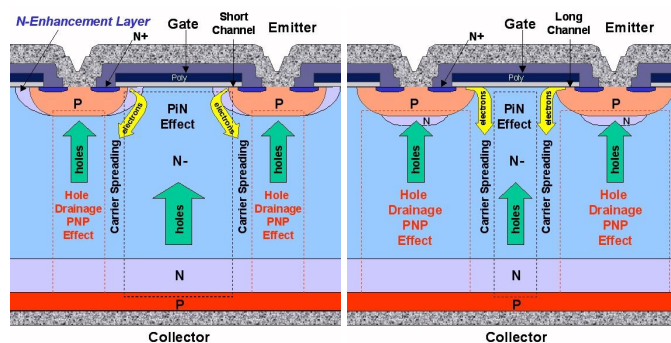
tion is, the stronger the enhancement effect will be accompanied with a reduced breakdown voltage. The enhancement n-layer region has been employed effectively in both planar [6] and trench [7] IGBTs as shown in Figure 3. For both designs, the n-layer fully surrounds the p-region, with the sole task of storing holes, or in other words preventing them from penetrating into the p-region (hole-barrier). However, for planar structures, the n-layer plays a more interacting role depending on its positioning and doping profile. Hence, with further optimization, an enhanced planar cell performance can still be made to rival that of today’s trench cell designs.



(a) Planar with n-layer (b) Trench with n-layer and dummy cells
Fig. 3: Planar (a) and Trench (b) IGBT with n-layer.

III. ENHANCED-PLANAR TECHNOLOGY

In order to design the enhancement n-layer for an optimum trade-off between low losses, high SOA and maximum blocking capability, the positioning and doping profile of the n-layer was investigated experimentally. Results were also confirmed through simulations carried out on the different structures. In addition to an n-layer fully surrounding the cell’s p-well, prototype samples were fabricated where an n-layer was only placed laterally near the edge of the p-well, and in a third version it was centralised underneath the p-well as shown in Figure 4. The peak concentration for the n-layer was the same for all three versions.



(a) Lateral n-layer (b) Centralised n-layer
Fig. 4: Planar IGBT with a lateral (a) and centralised (b) n-layer during conduction.

Major improvements in on-state losses were observed for the lateral version, similar to those achieved for the fully encompassed p-well structure. This was attributed to three main interacting effects; 1) an improved spreading of electrons from the MOS channel, 2) a shorter channel length, and 3) an improved

PiN effect between the cells due to the enhanced hole-accumulation at the periphery of the cell. Due to the fact that the lateral n-layer does not extend beyond the maximum p-well depth, a favourable trade-off with blocking capability was achieved, thus allowing a higher doping for the enhancement n-layer to obtain even lower losses. These effects were all absent in the second centralised version, which only provided a hole-barrier under the cell with a negligible contribution to plasma enhancement. However, the centralised n-layer design demonstrated a higher RBSOA capability compared to the other structures due to the positioning of the peak field directly below the contact. This was achieved at the expense of reduced blocking voltage capability. The final EP-IGBT design utilised an optimum doping profile for both the lateral and centralized regions for achieving the lowest on-state losses, maximum blocking capability and highest SOA limits. Remarkably, cosmic ray measurements have also shown that the EP-IGBT does not result in a higher failure rate of at the required DC voltage levels when compared to the equivalent standard IGBT.

IV. 6.5kV EP-IGBT ELECTRICAL CHARACTERISTICS

Technology Benchmark: To demonstrate the low loss electrical performance of the new technology, a 25A/6500V EP-IGBT chip was measured for the static and dynamic characteristics. At 25A, the EP-IGBT chip was operating at a current density of 30A/cm². The correlation obtained by plotting E_{off} versus V_{ce(sat)}, strongly depends on the manufacturing technology. A simultaneous decrease of both parameters was achieved by the improved Enhanced-Planar technology as shown in Figure 5 for the 6500V chip. The V_{ce(sat)} is reduced from 5.4V to 3.7V for the EP-IGBT, representing approximately a 30% drop in on-state losses compared to the standard device while keeping the same E_{off} value.

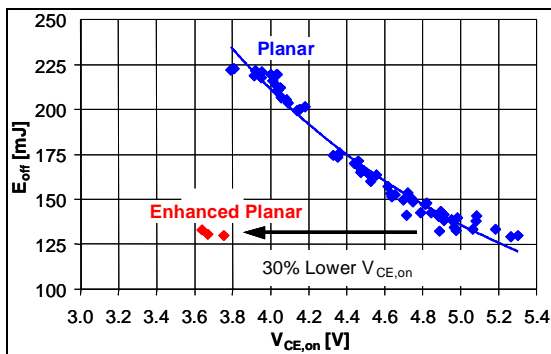


Fig. 5: 25A/6500V EP-IGBT losses trade-off benchmark.

Static Characteristics: The on-state characteristics are presented in Figure 6 showing that the chips exhibit a good positive temperature coefficient even at low current densities for safe paralleling.

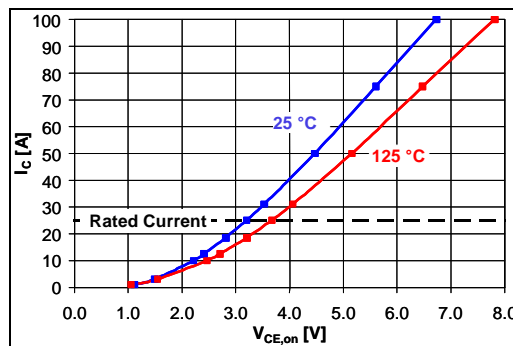
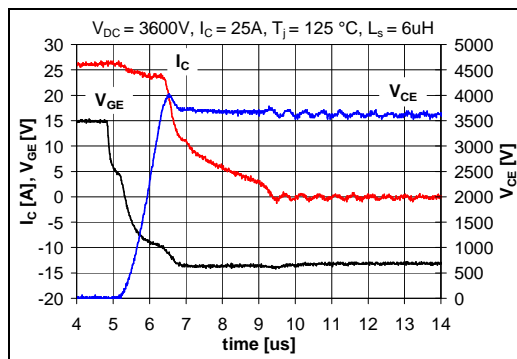
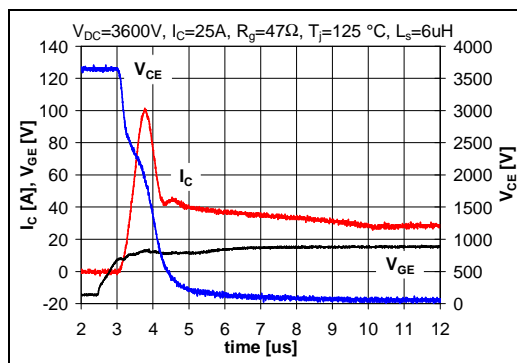


Fig. 6: 25A/6500V EP-IGBT on-state characteristics.

Dynamic Characteristics: One of the main goals of the new technology development was to achieve the low on-state losses without sacrificing the device soft switching behaviour and the benchmark robust performance. Due to the same silicon design, SPT buffer and planar design, these goals were met or even exceeded for the RBSOA despite of the improved technology curve. Figure 7a and 7b show the turn-off and turn-on waveforms respectively at 125°C under nominal conditions while employing a high stray inductance value of 6µH.



(a) Turn-off current and voltage waveforms.



(b) Turn-on current and voltage waveforms.

Fig. 7: 25A/6500V EP-IGBT nominal switching waveforms.

The turn-off losses E_{off} were kept low at a value of 130mJ using a gate resistance value of 33ohms. Therefore, a perfect balance is achieved resulting in fast switching speeds with low losses, short tail current, low overshoot voltage and low EMI levels. The IGBT was also designed to obtain low turn-on switching losses E_{on} due to an optimised input capacitance for faster V_{ce} fall times combined with a suitable diode. The turn-on losses have typical values of 150mJ under nominal conditions at

125°C and a di/dt value of 160A/μsec using a gate resistance value of 47ohms.

RBSOA Performance: The RBSOA turn-off at 125°C was carried out at a current level of 95A (> 3 times nominal) and a dc-link voltage of 4500V as shown in Figure 8. Using a low gate resistance value of 33ohms, the device clearly maintains high immunity against strong dynamic avalanche under these extreme conditions. An extremely rugged IGBT offers the possibility of operating the device with significantly lower gate-resistance values (R_{Goff}) resulting in shorter delay times during device turn-off for improving the current sharing between paralleled IGBTs. Furthermore, in order to examine the device capability to withstand Switching-Self-Clamping-Mode SSCM [1], the EP-IGBT was tested at a current level of 105A (> 4 times nominal) at a dc-link voltage of 4500V with an even larger stray inductance of 14μH. No external gate resistance, active clamp or snubber was employed in the test circuit. Figure 9 shows the EP-IGBT self-clamping the overshoot voltage successfully at 6500V.

pulse of 12μsec. Controllable and clean current waveforms were obtained exhibiting no parasitic oscillations thanks to the combination of an optimal EP-IGBT cell and SPT design. The SPT buffer and anode designs employed in the EP-IGBT have been optimised in order to obtain a high short-circuit SOA capability, even withstanding the short circuit conditions at gate voltages exceeding 15V.

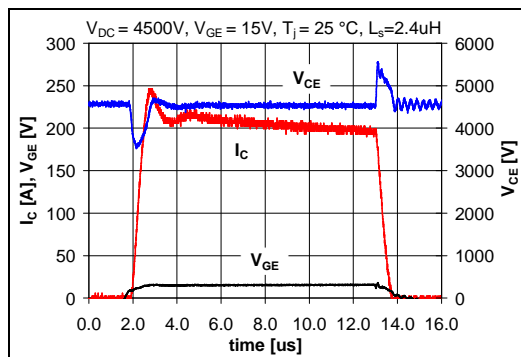


Fig. 10: 25A/6500V EP-IGBT short circuit waveforms.

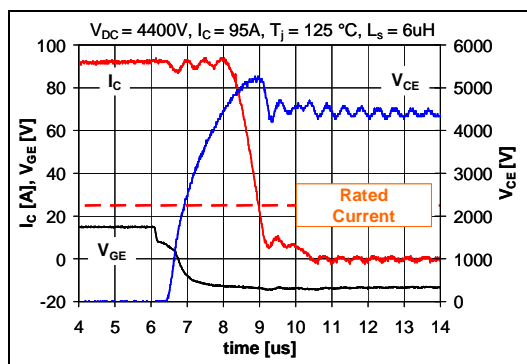


Fig. 8: 25A/6500V EP-IGBT RBSOA turn-off.

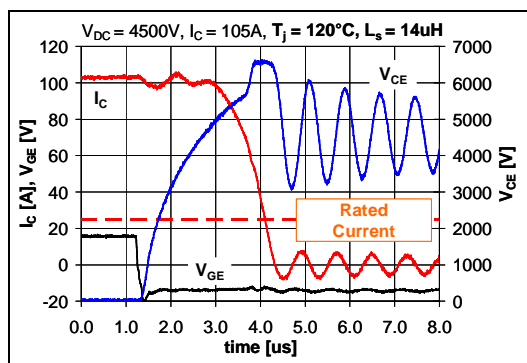


Fig. 9: 25A/6500 V EP-IGBT RBSOA turn-off with SSCM.

By enabling the IGBT to withstand SSCM, the device will exhibit a square SOA capability up to the self-clamp voltage level. The high dynamic ruggedness and SSCM capability, combined with smooth switching behaviour will provide users with greatest margins for optimising the design of their systems.

Short Circuit Performance: The high short-circuit capability of the new EP-IGBT was also demonstrated at 25°C as shown in Figure 10. The waveforms show the 25A/6500V EP-IGBT in short-circuit mode at a dc-link voltage of 4500V for a current

V. CONCLUSION

Compared to existing state-of-the art IGBTs, the newly developed Enhanced-Planar IGBT achieves 15-30% lower on-state losses while still maintaining low turn-off losses, thereby setting a new technology benchmark especially for high-voltage IGBTs. The world's first low-loss 6.5kV EP-IGBT prototype was presented with a $V_{ce(sat)}$ value well below 4V while achieving the same very high SOA and SSCM capability during switching as with the standard technology. The electrical characteristics demonstrate that the planar technology can match trench technology in terms of cell enhancement for lower losses while maintaining its SOA superiority. By utilizing the lower losses in high voltage systems, a 10%-20% increase in the total output current is predicted without any changes in the inverter design.

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