Freewheeling Diode Reverse Recovery Failure Modes in IGBT Applications

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Abstract- **In this paper, reverse recovery failure modes in modern fast power diodes are investigated. By the aid of semiconductor device simulation tools, a better view is obtained for the physical process, and operating conditions at which both diode snappy recovery and dynamic avalanching occur during the recovery period in modern high frequency power electronic applications. The work presented here confirms that the reverse recovery process can by expressed by means of diode capacitive effects which influence the reverse recovery characteristics. The paper also shows that the control of the carrier gradient and the remaining stored charge in the drift region during the recovery phase influence both failure modes and determine if the diode exhibits a soft, snappy or dynamic avalanche recovery characteristics.**

I. INTRODUCTION

THE RISE of the converter frequency in power electronics requires fast power semiconductor devices with low switching losses during the transient periods. Today, Mos-Bipolar Transistors such as the (IGBT) present interesting characteristics combining both MOS and bipolar structures to achieve a voltage driven device with low on-state losses, low switching losses and a high current density capability. These devices are increasingly used in many modern converter applications, but their optimum performances are often restricted by the freewheeling diode reverse recovery characteristics.

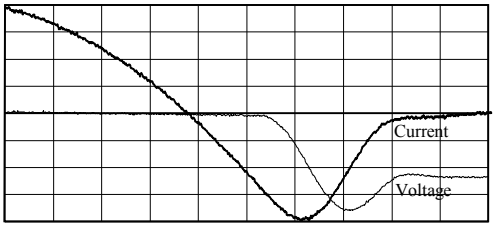
The freewheeling diode has always been said to be the weak component in many applications because it reduces the switching speed of the IGBT during the turn-on transient period. The main two reverse recovery failure modes in diodes operating under high stress condition are

1- Snappy Recovery.
2- Reverse Recovery Dynamic Avalanche.

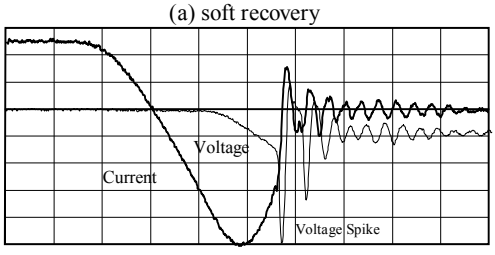
One of the most common and catastrophic failure modes in fast diodes is due to diode snappy recovery. Previous work have shown that under adverse combinations of high commutating *di/dt*, large circuit stray inductance, low forward current and low junction temperature, it is likely that all fast power diodes produce excessive voltage spikes due to snappy recovery [1]. This in turn can destroy the diode and ultimately cause a circuit failure due to excessive inrush duty in the recovery period. Experimental results are shown comparing a desirable soft recovery performance in figure (1-a) to snappy recovery in figure (1-b).

Snappy recovery of fast power *PIN* diodes has been investigated over the years [2]. These studies have shown that the depletion of the remaining stored charge during the recovery period results in a current discontinuity (chop-off). This produces a very high di_r/dt and hence a large voltage overshoot which may result in the destruction of the device.

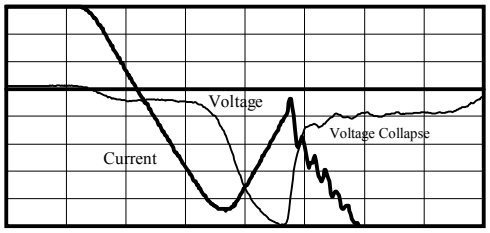
The second type of failure mode, termed as reverse recovery dynamic avalanching occurs at high *di/dt* switching speeds. Normally, the process itself is safe if the device does not exhibit any non-uniformaties in the recovery current. However, dynamic avalanching can result in the generation of a hot spot in the silicon die due to non-uniform current crowding leading to the distruction of the device as shown in figure (1-c). The causes of these hot spots can range from process to material variations in a single diode silicon chip. To prevent this failure mode, certain design/process consideration must be taken into account to minimise the effects of any current non-uniformaties.



(a) soft recovery



(b) snappy recovery



(c) dynamic Avalanche

Fig. 1 Reverse recovery waveforms for a fast diode, (a) soft recovery, (b) snappy recovery and (c) dynamic avalanching. These diode failure modes can destroy the IGBT and ultimately cause a circuit failure due to excessive inrush duty in the recovery period as shown in figure (2). The purpose of this investigation is to gain a better understanding of the physical process, and causes of these failure modes in modern fast power diodes.

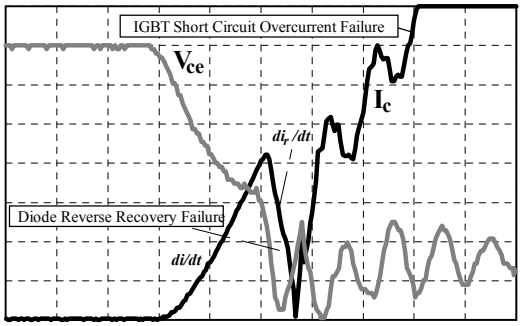
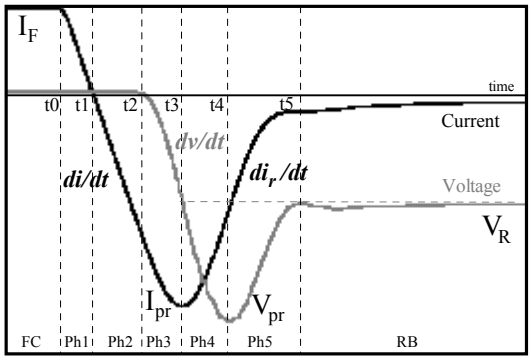


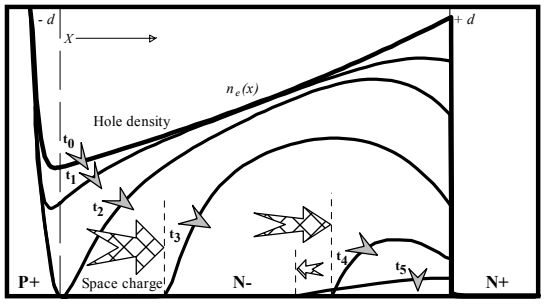
Fig. 2 Freewheeling diode reverse recovery failure during IGBT turn-on.

II. DIODE REVERSE RECOVERY PROCESS

Figure (3-a) shows typical diode current and voltage waveforms during reverse recovery, while figure (3-b) shows the associated excess minority carrier distribution (hole density) and space charge spreading in the drift region during reverse recovery.



(a) Diode reverse recovery voltage and current waveforms.



(b) Excess carrier distribution during reverse recovery.

Fig. 3 Reverse Recovery Characteristics (a) with the associated excess minority carrier distributions (b).

During Forward Conduction *FC*, the diode conducts a constant steady state forward current *IF*, and a fixed forward voltage drop *Vf* appears across the diode.

An increase in the diode current will lead to an increase in the number of excess minority carriers associated with a larger conductivity modulation in the drift region. The current flows only due to recombination and generation processes where the total stored charge in the drift region is a function of the current density, carrier lifetime, junction temperature and carrier injection efficiency. The excess minority carrier distribution in the drift region [3] is given as

$$n_e(x) = \frac{I_F \tau_a}{2qA_{eff} L_a}\left[\frac{\cosh(x/L_a)}{\sinh(d/L_a)} - B\frac{\sinh(x/L_a)}{\cosh(d/L_a)}\right] \quad (1)$$

where the boundary conditions are given as

$$(-d\big|_{p^+n^-} \le x \le d\big|_{n^-n^+}.) \quad (2)$$

La is the ambipolar diffusion coefficient, τa is the ambipolar lifetime value, B is the hole to electron mobility ratio (B≈3) and ($d=W_B/2$) where W*B* is the drift region total thickness.

When the diode is subjected to a reverse voltage *VR* at $t = t_0$, a certain reverse recovery transient period elapses before the diode can reach its full Reverse Blocking *RB* state. This period can be divided into five phases :

Phase 1 (Commutating Phase): This phase begins with the application of the reverse voltage *VR* at $t = t_0$. The current drops at a rate *di/dt* until it reaches the zero crossing point at $t = t_1$. This phase is fully dependent on the circuit components, where the commutating *di/dt* is mainly a function of the reverse voltage, circuit inductance and the IGBT gate circuit components.

Phase 2 (Storage Phase): This phase starts after $t = t_1$ as the current turns negative. The phase ends at $t = t_2$ when the total excess carrier concentration at the p^+n^- junction is reduced to zero.

Phase 3 (Voltage build-up Phase): This phase marks the start of the *recovery period* at which the depletion region starts to form across the p^+n^- junction sweeping out the remaining excess carriers from the drift region. The voltage across the diode will increase at a rate *dv/dt* as the depletion region widens, until it reaches the value of the applied voltage V_R at $t = t_3$. Hence at that point *di/dt=0* and the diode current reaches its peak value *Ipr*.

Phase 4 (Inductive Phase): This phase starts when the recovery current begins to fall from its peak value *Ipr*, while the voltage continues to increase until it reaches the peak value V_{pr} at $t = t_4$.

Phase 5 (Recovery Phase): The final phase starts when the voltage begins to fall reaching its steady state reverse blocking value at $t = t_5$, while the current continues to drop to its leakage level. The failure modes under investigation normally occur during this phase and are mainly dependent on the remaining excess carriers near the n^-n^+ junction. In the following sections, a detailed analysis of each phase is presented

i) Phase 1 and Phase 2 (Storage Period)

By assuming an ideal switch the diode current drops at a rate (*-di/dt*) at the start of the reverse recovery period where

$$\frac{di}{dt} = -\frac{V_R}{L_c} \tag{3}$$

therefore the diode current can be given as

$$i(t) = I_F - (V_R / L_c)t \tag{4}$$

The inductance *Lc* supports the full reverse voltage, while the diode voltage drop will maintain the same value *Vf* as long as there is a sufficient stored charge at the junction. The diode current also stays positive as long as $I_F > (V_R / L_c)t$ reaching its zero crossing point at $t = t_1$.

At the start of phase 2, the current becomes negative when $I_F < (V_R / L_c)t$ but continues to drop at the same rate. The diode voltage drop falls slightly from its normal value, and the voltage remains supported by the circuit inductance until $t = t_2$ when the excess carriers near the junction edge are reduced to their equilibrium values. The rate of reduction in carrier density (*-dn/dt*) is described by the continuity equation. The time during this phase is known as the storage period $t_s = t_2 - t_1$ where

$$i(t_s) \approx (V_R / L_c)t_s \tag{5}$$

The storage time is dependent on both external operating parameters and diode structure. The reduction of the stored charge during phase 1 and 2 can be described by the charge control equation.

$$\frac{dQ}{dt} = -i(t) - \frac{Q(t)}{\tau_{eff}} \tag{6}$$

which illustrates that the rate of change of the stored charge *dQ/dt* is due to internal recombination and the charge being swept out of the drift region due to the reverse recovery current. The swept out charge during the storage phase is also known as the storage charge.

ii) Phase 3 and Phase 4 (Capacitive Effects)

When the total excess carrier concentration at the p^+n^- junction is reduced to zero, the depletion region starts to form sweeping out the remaining excess carriers from the drift region. The voltage across the diode will begin to build up at a rate *dv/dt* as the depletion region widens. At this point, two dominant charge storage effects control the reverse recovery characteristics. The first effect takes place as the voltage across the diode increase, associated with an increase in the depletion region width *Wd*. This implies a change in the charge within the depletion layer to balance the change in the junction voltage. The magnitude of the total charge on either side of the junction is the depletion layer charge *Qd*, which is associated with the junction capacitance C_j where

$$C_j = \frac{dQ_d}{dV} \tag{7}$$

the current flowing through this capacitor is called the displacement current $i_d(t)$

$$i_d(t) = C_j^* \frac{dV}{dt} \tag{8}$$

assuming an average constant value for the junction capacitance C_j^{**} for simplicity. The second effect is the stored charge *Q(t)* left in the bulk of the drift region after $t = t_2$. This charge effect is reduced during the recovery period either by recombination $Q_r(t)$ or by a drift current $i_D(t)$ due to the large electric field build up as the depletion layer penetrates deeper into the drift region. The charge associated with this current can be termed as the drift charge $Q_D(t)$ where

$$Q(t) = Q_r(t) + Q_D(t) \tag{9}$$

where

$$Q_D(t) = C_D v(t) \tag{10}$$

C_D is termed as the drift capacitance because the reduction in charge is due to a drift current and can also be given as

$$C_D = \frac{dQ_D}{dV} \tag{11}$$

The total recovery current flowing through the diode is

$$i_R(t) = i_d(t) + i_D(t) \tag{12}$$

therefore the charge control equation can be given as

$$\frac{dQ}{dt} = -i_R(t) - \frac{Q(t)}{\tau_{eff}} \tag{13}$$

hence

$$\frac{dQ}{dt} = -i_D(t) + C_j^* \frac{dv}{dt} - \frac{Q(t)}{\tau_{eff}} \tag{14}$$

From equation (10), and assuming $C_D(t)$ as a time dependent variable, we can write:

$$i_D(t) = \frac{dQ_D}{dt} = C_D \frac{dv}{dt} + \frac{d}{dt}\left(\frac{dQ_D}{dv}\right)v(t) \tag{15}$$

where

$$i_D(t) = C_D \frac{dv}{dt} + g_D(t)v(t) \tag{16}$$

$g_D(t)$ represents a time dependent conductance for the diode during recovery, where it can also be expressed as dC_D/dt, therefore the total recovery current can be given as

$$i_R(t) = (C_j^* + C_D)\frac{dv}{dt} + g_D(t)v(t) \tag{17}$$

This equation describes the variation of the diode recovery current in which the diode can be represented by a conductance $g_D(t)$ in parallel with two capacitors C_D and C_j^* as shown in figure (4) for a typical reverse recovery RLC circuit. From this diode model and circuit, equations governing the diode current and voltage characteristics during reverse recovery can be derived.

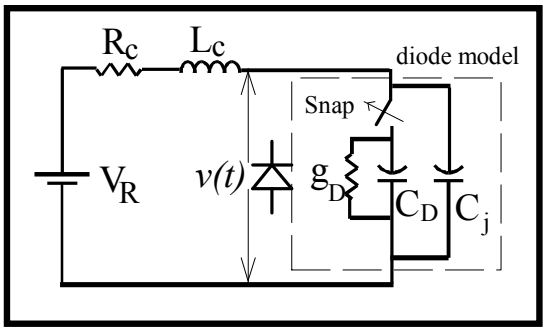


Fig. 4 Diode dynamic model in an RLC circuit.

At the beginning of phase 3, the current rate of change becomes both circuit and device dependent and is termed di_r/dt in the following analysis. By applying KVL we obtain

$$v(t) = V_R - L_c \frac{di_r}{dt} - R_c i_R(t) \tag{18}$$

therefore

$$\frac{di_r}{dt} = \frac{V_R - v(t) - R_c i_R(t)}{L_c} \tag{19}$$

When $(v(t_3) - i_R(t_3)R_c = V_R)$, the diode current reaches its maximum peak value *Ipr* at $t = t_3$ and $(di_r/dt=0)$. Also by rearranging (17), *dv/dt* can be given as

$$\frac{dv}{dt} = \frac{i_R(t) - g_D v(t)}{C_j^* + C_D} \tag{20}$$

At the start of Phase 4, di_r/dt becomes positive. This induces a positive voltage across the circuit inductance which adds to the applied reverse voltage. Thus the diode voltage continues to increase where

$$v(t) = V_R + L_c \frac{di_r}{dt} - R_c i_R(t) \tag{21}$$

By differentiating (16) and (21) and by replacing di_r/dt and *dv/dt* by their equivalents in (19) and (20), second order differential equations for both the diode recovery current and voltage can be obtained by assuming constant values for both C_D and g_D

$$\frac{d^2v}{dt^2} + \frac{R_c(C_T) + g_D L_c}{L_c(C_T)}\frac{dv}{dt} + \frac{1 + R_c}{L_c(C_T)}v(t) = \frac{V_R}{L_c(C_T)} \tag{22}$$

and

$$\frac{d^2 i_r}{dt^2} + \frac{R_c(C_T) + g_D L_c}{L_c(C_T)}\frac{di_r}{dt} + \frac{1 + R g_D}{L_c(C_T)}i_R(t) = \frac{g_D V_R}{L_c(C_T)} \tag{23}$$

where $C_T = C_j^* + C_D$.

Therefore, the average damping ratio ζ^{**} for the system was found to be equal to

$$\zeta^* = \frac{(C_T) + g_D L_c}{2\sqrt{L_c (C_T)(1+g_D)}} \quad (24)$$

Thus, the value of the damping factor can become an indicator of for the type of recovery the diode exhibits in the following phase. Phase 4 ends when the voltage reaches its maximum value V_{pr} at the maximum di_r/dt where

$$V_{pr} = V_R + L_c \left.\frac{di_r}{dt}\right|_{MAX} \quad (25)$$

iii) Phase 5 and Failure Modes

The transient behavior in the final phase can be explained using the damping ratio given in equation (24). Three types of recovery can normally be distinguished dependent on the device and operating conditions as shown in figure (5).

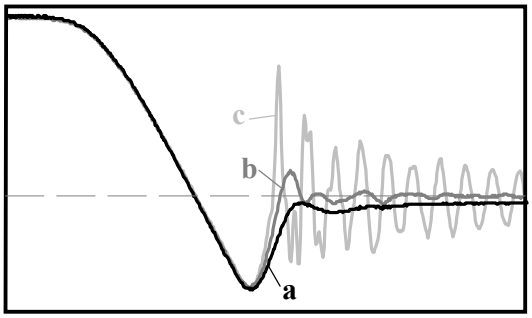


Fig. 5 Diode current waveforms showing three types of recovery (a) Soft, (b) Oscillatory and (c) Snappy.

(a) If the drift region contains a sufficient amount of carriers, then $C_D >> C_j^*$*, and $g_D < 1$. The drift capacitance dominates the recovery characteristics and ζ^**≥1. A soft recovery current tail is produced and the current decays with a low di_r/dt, and ζ^{**} can be approximated as

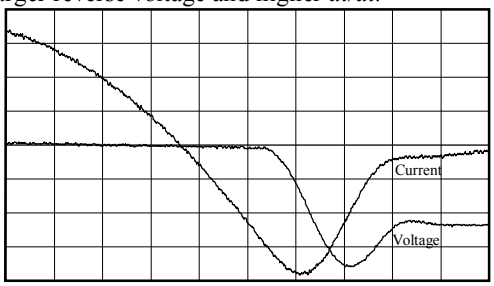
$$\zeta^* \approx \frac{1}{2}\sqrt{\frac{C_D}{L_c}} \quad (26)$$

(b) If the number of carriers is relatively small at the peak recovery voltage, then the recovery current will subsequently fall rapidly causing an oscillatory recovery waveform. This tends to occur in the underdamped case, where 0<ζ^**<<1 for low values for C_D.

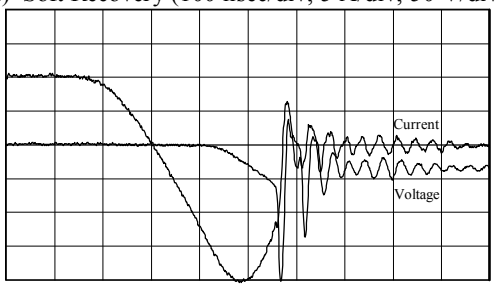
(c) If the voltage reaches a certain critical value during phase 4 causing a rapid reduction in minority carrier concentration, the diode then becomes snappy. Normally, this occurs prior to the diode normal inductive overshoot voltage. In this case, C_D=0, which can be approximated to an ideal undamped case $\zeta^* \approx 0$, and the junction capacitance become the dominate parameter in the recovery characteristics

$$\zeta_j = \frac{1}{2}\sqrt{\frac{C_j^*}{L_c}} \quad (27)$$

Since C_j^** has a very small value compared to C_D (see below), a large *dv/dt* is required to maintain the value of the reverse recovery current. A large *dv/dt* cannot be sustained constantly and therefore a rapid decrease in the recovery current occurs. The current appears to chop-off producing a large di_r/dt, and subsequently a large $L_c(di_r/dt)$ voltage spike across the diode. Experimental results presented in figure (6-a) shows soft recovery characteristics for the diode tested for a low *di/dt* and low reverse voltage, while figure (6-b) shows snappy recovery at a larger reverse voltage and higher *di/dt.*



(a) Soft Recovery (100 nsec/div, 5 A/div, 50 V/div).



(b) Snappy Recovery (100 nsec/div, 10 A/div, 300 V/div).

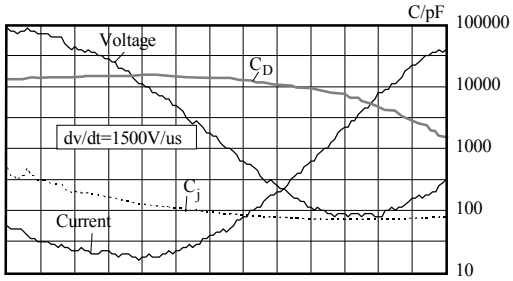
Fig. 6 Reverse recovery experimental results for a fast recovery diode, (a) Soft recovery and (b) Snappy recovery.

From the experimental results shown in figure (6), figure (7) shows expanded diode voltage and current waveforms during the diode recovery phase. In order to confirm the previous analysis, the reverse recovery charge Q_{rr} which represents the stored charge being swept out of the drift region during the recovery period (t_r) is calculated by integrating the recovery current over the recovery period. By differentiating the charge with respect to voltage, where both are functions of time, a curve for C_D is plotted as shown in figure (7) for both the soft and snappy recovery waveforms. Also measurements of the steady state junction

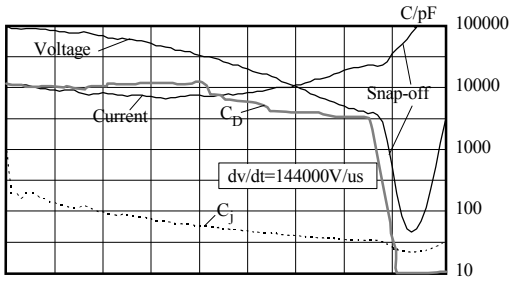
capacitance C_j^** for the diode have been obtained using an LCR meter. These measurements were in good agreement with the calculated values for the average C_j^** of an abrupt junction

$$C_j^* = \frac{1}{V_2 - V_1} \int C_j(v)dv \tag{28}$$

where V_1 and V_2 are the limits over which the voltage across the diode varies. A curve for C_j^** is also plotted in figure (7) to compare both capacitive effects during diode recovery. For simplicity, the effect of approximating the junction capacitance to an average value was found to be negligible. Also C_D can be treated as a constant before the voltage starts to increase and the charge begins to drop. Normally for the soft recovery case, C_D would dominate the recovery characteristics having a larger value. Eventually for the snappy case, the charge disappears as the voltage reaches the critical value. Therefore, C_D drops rapidly to zero, and the only capacitance left is junction capacitance C_j^** having a very low value around *100pF* compared to C_D having a value of *10nF* before snap-off .



(a) Soft recovery (100nsec/div, 250V/div, 5A/div).



(b) Snappy recovery (100nsec/div, 250V/div, 5A/div).

Fig. 7 Current, Voltage, C_D and C_j^** waveforms during the recovery phase, soft recovery (a), snappy recovery (b).

III. CAUSES OF SNAPPINESS IN DIODES

Power semiconductor device design rules have always been aimed at achieving the optimum trade-off curves between the on-state losses, switching losses and the required blocking capability. However, snappy recovery forces an added requirement in the design of fast power diodes in order to achieve soft recovery characteristics. The main goal is to prevent the sudden disappearance of the remaining carriers during the recovery phase. Snappy recovery is in fact dependent on all circuit and diode design parameters as presented in the block diagram shown in figure (8).

These parameters provide different mechanisms which affect the amount and position of the rest charge left at the end of the storage phase. This in turn influences the recovery di_r/dt as shown from the previous analysis and subsequently determine the value of the inductive voltage overshoot. By exceeding a critical value (V_c), snappy recovery occurs causing the diode to produce destructive voltage spikes.

In order to study the effects of both device and operating condition parameters, it is necessary to outline the principles of the minority carrier distribution profile and its effect on the reverse recovery behavior.

From figure (3-b) and equation (1), we can determine the excess carrier concentration at each end as

$$n_e(-d)\big|_{p^+n^-} = \frac{I_F \tau_a}{2qAL_a}\left[\coth(d/L_a) + B\tanh(d/L_a)\right] \tag{29}$$

also

$$n_e(+d)\big|_{n^-n^+} = \frac{I_F \tau_a}{2qAL_a}\left[\coth(d/L_a) - B\tanh(d/L_a)\right] \tag{30}$$

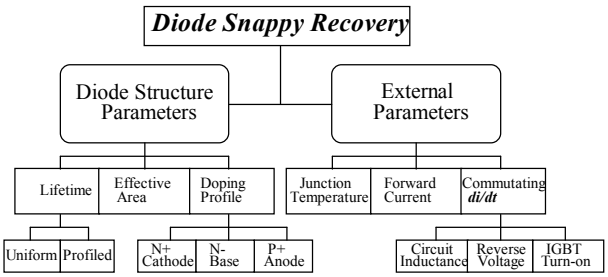


Fig. 8 Diode and circuit parameters effecting snappy recovery.

The asymmetrical carrier distribution arises because of the unequal values of the electron and hole mobilities. Also the reduction in the minority carrier concentration near the p^+n^- junction is more rapid when compared to the other end. A ratio *K* for the excess carrier concentration at each junction can be defined as

$$K = \frac{n_e(pn^-)}{n_e(n^-n^+)} = \frac{n_e(-d)}{n_e(+d)} \tag{31}$$

The gradient of the excess carrier concentration is approximated as

$$\frac{dn_e}{dx} = \frac{n_e(-d) - n_e(+d)}{W_B} \tag{32}$$

Therefore the excess carrier concentration profile plays the main role in determining the shape of the reverse recovery characteristics [3]. In addition, the critical voltage V_c is a function of the drift region parameters and the excess carrier profile. This is due to their influence on the depletion layer spreading during reverse recovery.
Two different mechanism are observed by which the depletion layer removes the excess carriers from the drift region

1) *One Sided Penetration of the depletion layer* removing the excess carriers from one end if (K<1) or (K=1 for a large excess carrier concentration).
2) *Two sided Penetration of the depletion layer* removing the excess carriers from both ends (K>1) or (K=1 for a shallow excess carrier concentration).

For a one sided penetration, normally the critical voltage is approximated to the static punch-through voltage for a *PIN* structure, which is mainly dependent on the drift region thickness and doping level. However, under dynamic conditions, an excess carrier profile with (K<1) tends to slow down the spreading of the depletion layer. This increases the punch-through voltage results in soft recovery characteristics unless the inductive overshoot is still large enough due to higher *di/dts* or larger stray inductances. This type of profile can be achieved using lower emitter efficiency [4] or profiled lifetime control techniques [5] both of which have an added advantage in reducing the reverse recovery charge. The value of the punch - through voltage can also be increased by increasing the drift region thickness or doping concentration [6]. Other novel techniques include the use of buffer layers or deep diffused N^+ layers [7].
For a two sided penetration, the critical value is reduced below the static punch-through voltage and the diode exhibits a snappy behavior. This normally happens at low current densities, low temperatures, low uniform lifetime values and using high injection efficiency emitters.
Simulation runs were performed to show the effect of the excess carrier concentration profiles resulting from varying different parameters in the diode structure on the reverse recovery performance.

IV. DIODE SIMULATION MODEL

To analyse the diode reverse recovery characteristics, device simulations were carried out using the *ISE|TCAD* semiconductor device simulation package. The *PIN* diode model doping profile and the ramp circuit model used in performing the transient simulations are shown in figure (9).

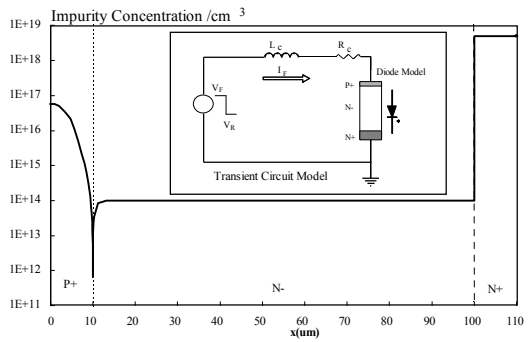


Fig. 9 Doping profile for the $p^+n^-n^+$ diode model including the transient circuit diagram.

For the diode model, a reference set of parameters were chosen. The P^+ emitter doping level at the anode contact is $(5\times10^{16}/cm^3)$. A gaussian function was selected to set the diffusion pattern for the layer with a p^+n^- junction depth of 10μm. The drift region had a thickness of 90μm and a doping level of $(1\times10^{14}/cm^3)$. These values were chosen to achieve a blocking voltage of 1200V and a punch through voltage of 650V. The N^+ layer at the cathode contact had a constant doping level of $(5\times10^{18}/cm^3)$ with a thickness of 10μm. The minority carrier lifetime in the drift region was given a value of 200nsec and the effective area of the diode was set at $0.5cm^2$.
The transient simulation were carried out at a junction temperature of 300K using a ramp *RL* circuit model. The circuit inductance L_c was given a value of 0.5μH, while R_c had a value of 0.1Ω. The diode conducted a forward current of 20A which is then ramped by the application of a reverse voltage of 150V. The commutating *di/dt* is only controlled via the circuit inductance and supply voltage, therefore *di/dt* is equal to 300A/μsec. This circuit model is adequate for investigating the diode reverse recovery characteristics. However, it is important to note that in an IGBT converter circuit, *di/dt* is also influenced by the IGBT gate circuit components. This indicates that the reverse recovery process experience lower voltages during the storage phase than those in the recovery phase. This would lead to softer recovery characteristics for the diode when compared to the ideal switch case with the same applied reverse voltage. Therefore the RL ramp circuit model would provide us with the worst case for our purpose of investigation.
Finally, in order to show the effect of each parameter independently on diode snappiness, one parameter was varied at a time, keeping the rest of the parameters at their reference values.

V. SIMULATION RESULTS

Figure (10) shows the current and voltage waveforms for the diode with the reference set of parameters, while the second diode has the same specifications but with an increased P^+ emitter doping level of $5\times10^{17}/cm^3$. It is clear that snappiness occurs at higher doping levels, while

a softer recovery occurs at lower levels. A higher doping level will result in a higher concentration of minority carriers stored near the p^+n^- junction than on the n^-n^+ side as shown in Fig. (11-b). The total amount of stored charge is larger in this case, therefore a longer period is needed to clear the p^+n^- junction from these excess carriers, meanwhile this extra time will lead to an extra removal of carriers from the n^-n^+ side, causing the depletion layer to build up on both ends. This will lead to the disappearance of charge near the n^-n^+ junction which is crucial for soft recovery characteristics of the diode.

As can be seen in this case the amount of stored excess carriers is not necessarily important, but the shape and position of the carriers is vital to determine whether the diode will be snappy or soft. A one sided penetration of the depletion layer will provide a soft recovery. A conclusion can be reached here that increasing the gradient of the excess carriers stored in the drift region from the p^+n^- junction to the n^-n^+ junction will result in softer characteristics, reducing the possibility of a space charge region building up at both ends. Similar effects can be achieved using shallower P^+ emitters.

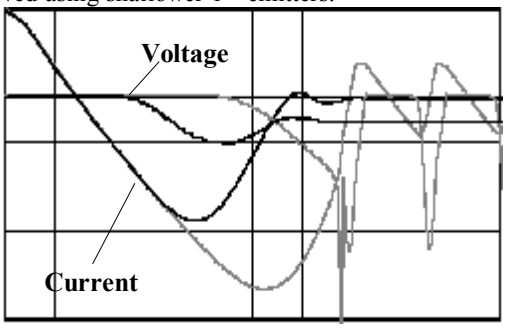
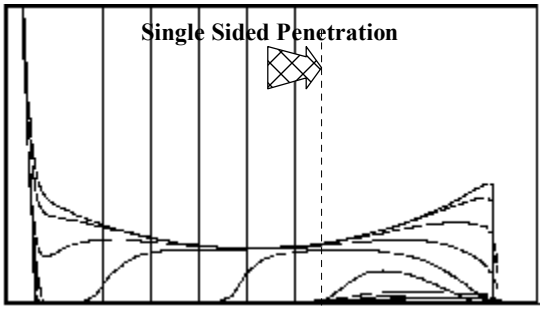
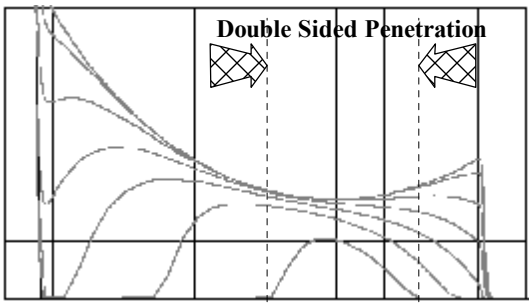


Fig. 10 Reverse Recovery Current and Voltage.
(10 A/div, 300 V/div, 50 nsec/div)
[Low P^+ Doping (Black), High P^+ Doping (Gray)]



(a) Low P^+ emitter doping.



(b) High P^+ emitter doping.

Fig. 11 Excess minority carrier distribution during reverse recovery
(50 nsec/step) (2.5×10^{16} / cm^3/div, 10 μm/div)

Figure (12) shows the voltage and current waveforms of two diode settings one with a very low lifetime value of 50nsec compared to the reference diode with 200nsec. Lower lifetime values results in a harder snappy recovery occurring at voltages lower than the punch-through value. In this case, the stored charge disappears when the depletion region starts to build up at both ends pushing the carriers into the middle of the drift region as shown in figure (13). A similar behavior is observed when the diode is operating at lower current densities or lower temperatures.

The punch through voltage can be varied by changing the drift region properties (thickness or doping). A thinner base region will result in a lower punch-through voltage. Figure (14) shows the reverse recovery characteristics for a snappy diode with a base width of 60μm compared to the reference diode with a 90μm base width. The case is similar for different base doping levels, but although the actual amount and shape of the stored carriers is not affected, the punch-through voltage will change. Therefore at lower doping levels, snappiness occurs due to a higher penetration of the depletion region at lower applied voltages. At high doping levels or non punch-through structures, the critical voltage is equal to the avalanche breakdown value.

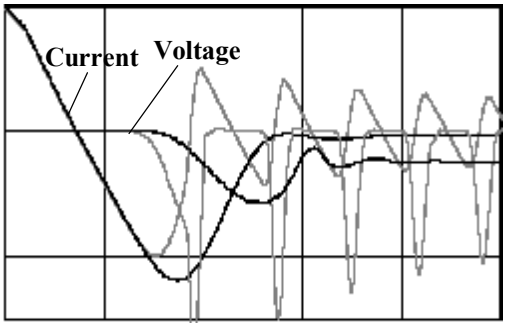


Fig. 12 Reverse Recovery Current and Voltage.
(10 A/div, 300 V/div, 50 nsec/div)

[High Lifetime 200nsec (Black), Low Lifetime 50 nsec (Gray)]

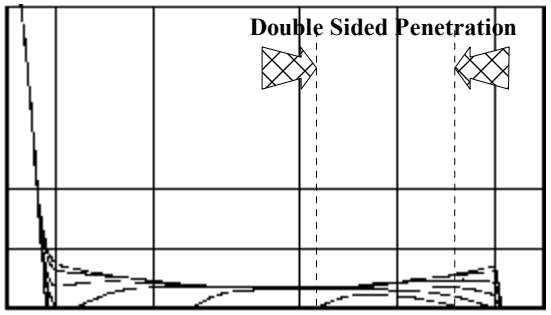


Fig. 13 Excess minority carrier distribution during reverse recovery for a lifetime of 50nsec *(50nsec/step)* (2.5×10^{16} / cm^3 / div, 10μm/div)

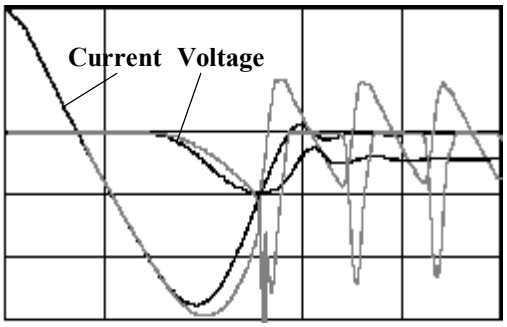


Fig. 14 Reverse Recovery Current and Voltage. (10 A/div, 300 V/div, 50 nsec/div)
[Thick Base 90μm (Black), Thin Base 60μm (Gray)]

VI. DYNAMIC AVALANCHING

Reverse recovery dynamic avalanching occurs when a diode suffers avalanche multiplication at values lower than the static breakdown voltage. Higher peak electric fields are present due to the excess minority carrier concentration in the drift region during reverse recovery. This can lead to an increase in the effective background doping N_{eff}, hence, generating extra amount of carriers and resulting in impact ionization. The process itself is stable if the extra generated holes and electrons are balanced in numbers and the current remains uniform across the device. Otherwise the process can get out of control leading to a device failure. N_{eff} is a function of the hole current density Jp [8] and the holes saturation velocity v_p and can be given as

$$N_{eff} = N_D + \frac{J_p}{qv_p} \qquad (33)$$

The reverse recovery SOA-IV curve can be provided [9] for a given chip area as shown in figure (15). Under normal operating conditions the IV curve should remain within the SOA limits. However, dynamic avalanching may occur if :

1) The reverse recovery IV curve exceeds the power dissipation capability of the chip (outside the SOA limits). This failure mode normally occurs at high forward currents, high temperatures, high reverse overshoot voltages and high di/dts.
2) The SOA curve is shifted due to very high current densities flowing in a small area of the device. This occurs due to material or process variations (Silicon dislocations, diffusions, lifetime killing, contact uniformity, etc.).

At typical operating current densities (100-200)A/cm^2, the second term on the right hand side of eq. (33) becomes irrelevant for doping concentrations above 1x10^{14}. Hence, for diodes with lower voltage ratings (<600V), this type of failure mode becomes less problematic. For higher voltage diodes (>1200V) with lower doping concentrations, the uniformity of the current in the diode during dynamic avalanching becomes very critical, and the second term dominate especially at very high *di/dt*s and reverse bias voltages.
Earlier, it was shown that during the recovery phase, all the holes near the n^-n^+ junction are swept out across the space charge. The high electric field barrier at that junction will also prevent the holes from diffusing into the *N*+ emitter. However, for the type of profile presented in figure (10-a), a hole diffusion element is introduced. The larger the remaining charge in the drift region during the recovery phase, the higher the diffusion current across the space charge region and we are more likely to experience dynamic avalanching. This extra charge will also prolong the recovery phase increasing the possibility of current crowding to form on the silicon chip.
An increase in the *P* emitter doping level will increase the injection efficiency at the pn^- junction and the hole diffusion current portion will be lower. This is likely to reduce the dynamic avalanche process with a lower risk of current non-uniformity and device failure.

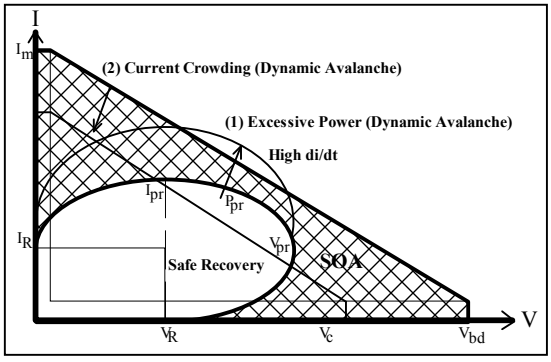


Fig. 15 Reverse Recovery Safe Operating Area in a Fast Diode.

VII. CONCLUSION

A detailed study of the reverse recovery snappy behavior in modern fast power diodes is presented in this paper. The analyses have shown that capacitive effects due to the

remaining stored charge in the drift region during the recovery phase will influence the recovery characteristics. Normally, for the soft recovery case, a large capacitance exists due to the stored charge in the drift region, hence, this capacitance dominates the recovery characteristics. A reduction in drift region thickness and/or carrier lifetime leads to the snappy recovery case, where the stored charge disappears as the voltage reaches the critical value. The only capacitance then remaining is the junction capacitance of the diode, and it is this discontinuity that causes the very large current and voltage oscillations and potentially destructive voltage spikes.

The interaction of the diode capacitance with the main circuit parameters is a key factor in determining the reverse recovery characteristics of a diode, and whether the diode adopts a soft or snappy recovery behavior for the given operating conditions and design.

Also, the gradient of the minority carrier concentration in the drift region plays a major role in the determining the shape and type of recovery. By ensuring that the excess carrier concentration during the forward conduction is greater near the n^-n^+ junction when compared to the p^+n^- junction, this helps to slow down the removal of charge and preventing the depletion layer from building up at both junctions during reverse recovery. At the same time, the higher gradient can degrade device ruggedness due to dynamic avalanching at higher *di/dt*s and reverse bias voltages. Both failure modes can be prevented through certain device/circuit design techniques in order to achieve a safe operating condition for the application.

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