A Family of Reverse Conducting Gate Commutated Thyristors for Medium Voltage Drive Applications

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Abstract

With the technological breakthrough of the Hard Driven GTO [1] many performance limiting thyristor trade-offs are no longer valid and a novel thyristor technology, the Integrated Gate Commutated Thyristor (IGCT) [2] emerged. Due to a transistor turn-off mode snubberless switching up to the avalanche limit is no longer an issue. Usable switching frequencies only limited by thermal considerations expand to the kHz range.

By implementation of the Transparent Emitter Buffer Layer technology [2] and a novel patented separation technique, monolithic integration of the thyristor and the anti-parallel freewheeling diode was achieved without any cumbersome compromises in diode performance. For state of the art diode turn-off performance lifetime tailoring by means of particle irradiation was used. An IGCT family specially developed for the demands of medium voltage drive inverters in the range of 0.5 to 6 MVA is presented and their characteristics are discussed.

Introduction

Development of GTO technology has led to a wide variety of applications in the range of 1 to 20 MVA, mainly adjustable speed drives [3,4] and railway interties [5]. Although these applications have proven the reliability and cost effectiveness of the GTO thyristor, there are still cumbersome disadvantages of this technology. The inhomogeneous switching mode of the GTO gives rise to the need for dv/dt limiting snubber capacitors and reduces the allowable switching frequency so that high voltage IGBTs are starting to raise competition even at the higher power levels [6]. The novel IGCT technology opens the unique possibility to join the turn-off ruggedness of the IGBT with the superior conduction properties of the thyristor.

The IGCT family presented in this paper features the following key properties:

- a wide range of applications is covered by 8 different devices in three voltage classes; maximum rated turn-off currents of 480 A to 3100 A (Vdc = 1.9 kV), 340 A to 2200 A (Vdc = 2.7 kV) and 275 A to 1800 A (Vdc = 3.3 kV)
- snubberless turn-off of maximum rated current at full dc-link voltage
- maximum switching frequency of more than 25 kHz limited only by thermal considerations
- Transparent Emitter Buffer Layer technology for lowest possible losses at rated capability to withstand cosmic radiation (< 100 FIT at full rated dc-link voltage)
- monolithically integrated freewheeling diode for reduced parts count.
- integration of semiconductor and gate driver for optimum performance and reduced system costs.

IGCT Technology

GCT Turn-off mode

The GCT turn-off mode is characterised by an extremely fast commutation of the cathode current to the gate (see fig. 1). The cathode emitter is turned off before the voltage at the main blocking junction rises. To achieve this, the whole cathode current is commutated to the gate within less than 1 µs. Any regenerative action from the GCT cathode which might lead to filamentation is therefore prevented, leaving just the p-base - n-base - anode emitter - pnp transistor active during turn-off. As well known from the IGBT, a transistor turn-off mode is very favourable for high turn-off ratings without a snubber.

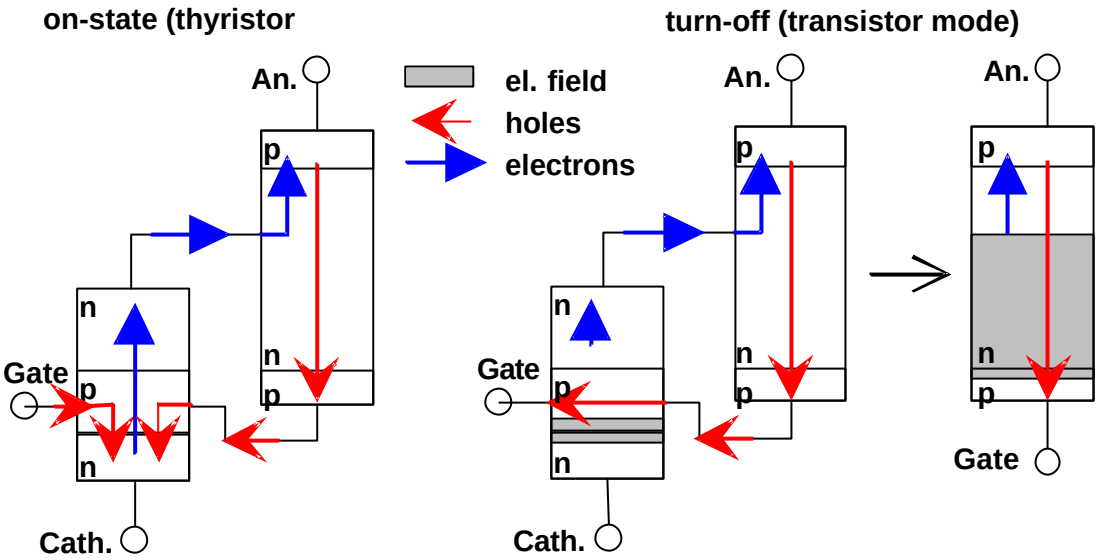

Fig.1: GCT-mode turn-off (two-transistor model)

Another important advantage inherent in the GCT turn-off mode is a strong reduction in turn-off time. Due to the high gate currents during commutation, the storage time is drastically reduced giving a total delay time from optical triggering of the gate driver to a voltage rise to 10% V_{dc} of only 3 µs. As the total variation of the turn-off time reduces to only 300 ns, series connection of GCTs is easily realised.

Generally it can be stated that the GCT switching is realised by forcing the thyristor into a transistor mode. This leads to a unique combination of the advantages of the thyristor and of the transistor.

Integrated Gate Drivers

The inductance of the standard packaging technology of GTOs in combination with a long coaxial cable to the gate driver would need a bulky and costly gate driver to the achieve the high di_{gate}/dt. This led to the development of the integrated gate driver concept: Novel low inductance GCT package are contacted directly to the GCT gate drivers, reducing the overall gate inductance to a value low enough to ensure the GCT switching mode with a single voltage source for blocking and turn-off. Additionally, the co-design of gate driver and GCT ensures best possible performance of the IGCT at lowest possible costs and energy consumption.

Finally, the IGCT is fed with a single dc current source allowing an uncomplicated design of the power supply. Triggering occurs by an optical input.

Buffer Layer Transparent Emitter Technology

Field experiences and long term blocking tests have shown in the past few years that cosmic radiation impact in combination with high electric field strengths can lead to instantaneous destruction of GTOs. For the standard GTO design the resulting need for lower electric fields leads to thicker devices which, in turn, led to higher on-state and switching losses. The GCTs are now consequently designed with a new technology, the *Buffer Layer Transparent Emitter* design, which gives a much better trade-off between the capability to withstand cosmic radiation and the silicon thickness [7, 8].

The Transparent Emitter technology uses a very thin anode emitter which allows part of the electrons to recombine at the contact metal interface - without generating holes. The emitter efficiency is, therefore, reduced without shorting the anode. The introduction of an n-buffer layer is now possible. As shown in Fig. 3 a trapezoidal distribution of the electric field can now be realised, which leads to a lower maximum field strength at even higher blocking voltages. Compared to a conventional GTO design silicon thickness can be cut by 1/3 giving even a higher capability to withstand cosmic radiation and cutting total losses to a minimum.

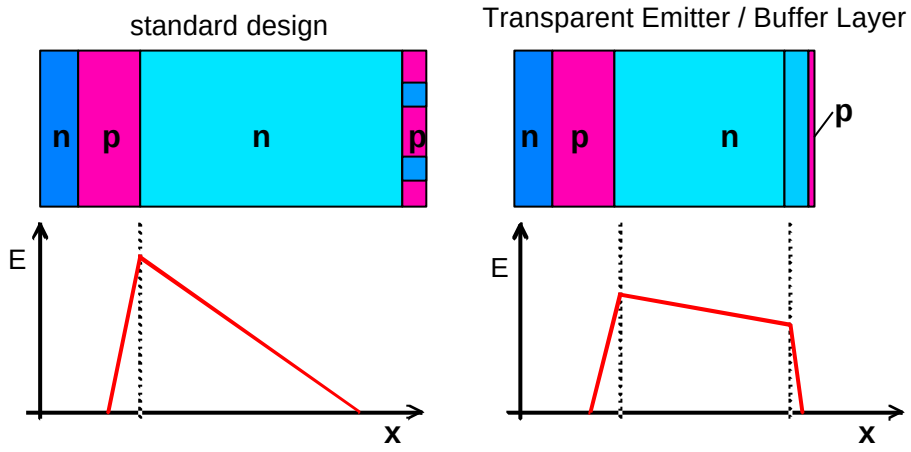

Fig.3: Comparison standard design/ transparent emitter buffer layer

Diode Technology

In the past, the advantages of monolithic reverse conducting GTOs were always offset by the fact that the GTO due to its conventional non punch-through design needed to be thicker than the optimum thickness for its corresponding freewheeling diode. Thus, reverse conducting GTOs suffered from excessive diode losses. With the transparent emitter buffer layer design this is no longer valid, the optimum thickness for both devices is now governed by the rated cosmic ray withstand capability which is the same for both. Additionally, the diode gets a cathode side n-buffer layer for free, which is known to enhance the turn-off behaviour.

Fig. 4 shows a schematic cross-section of a reverse conducting GCT. Special care must be taken at the boundary between diode and GCT. If the GCT p-base and the diode anode share a common blocking junction, an undesired resistive path between GCT gate and diode anode exists. This problem is addressed by a complete separation of both p-diffusion. The resulting pnp structure is designed to a blocking voltage of at least 20 V in each direction, preventing any significant current between GCT gate and diode anode.

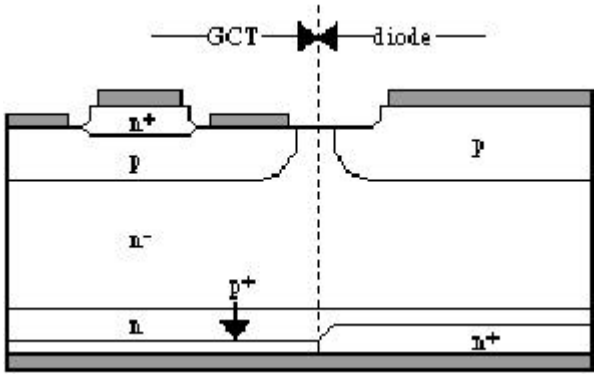

Fig.4.: Separation region between diode and GCT.

The diode turn-off behaviour is tailored by a combination of particle and electron irradiation giving a state-of-the-art trade-off between turn-off losses, reverse recovery current and on-state losses [9].

Device Rating

The following tables give an overview of the ratings and characteristics of the GCT family (turn-on losses are not listed as they represent less than one tenth of the turn-off losses). Fig. 5 depicts a photograph of the reverse conducting GCT family (the mechanical design of the gate drivers is still subject to changes).

			T_j = 0 - 115 °C $V_{dc\text{-}link}$ = 3300 V								
			GCT part				diode part				
Part n°	V_{DRM} [V]	$V_{dc\text{-}link}$ [V]	I_{tgqm} [A]	V_T [V]	E_{off} [J]	$\Theta_{jc,GCT}$ [K/W]	V_F [V]	di/dt [A/µs]	Irr [A]	E_{off} [J]	$\Theta_{jc,D}$ [K/W]
5SGX 03D6004	5500	3300	275	3.0	1.45	0.070		74	114		0.090
5SGX 06F6004	5500	3300	520	3.0	2.73	0.040		195	268		0.053
5SGX 10H6004	5500	3300	908	3.0	4.77	0.025		296	433		0.042
5SGX 19L6004	5500	3300	1815	3.0	9.54	0.012		533	781		0.021

Table 1: ratings and characteristic data of the 5.5 kV GCTs.

			T_j = 0 - 115 °C $V_{dc\text{-}link}$ = 2700 V / 1900 V								
			GCT part				diode part				
Part n°	V_{DRM} [V]	$V_{dc\text{-}link}$ [V]	I_{tgqm} [A]	V_T [V]	E_{off} [J]	$\Theta_{jc,GCT}$ [K/W]	V_F [V]	di/dt [A/µs]	I_{rr} [A]	E_{off} [J]	$\Theta_{jc,D}$ [K/W]
5SGX 04D402	4500	2700	338	3.0	1.33	0.070		113	107		0.090
	4500	1900	482	3.7	1.33	0.070		113	107		0.090
5SGX 08F4502	4500	2700	628	3.0	2.48	0.040		294	281		0.053
	4500	1900	894	3.7	2.48	0.040		294	304		0.053
5SGX 14H6004	4500	2700	1095	3.0	4.32	0.025		448	427		0.042
	4500	1900	1560	3.7	4.32	0.025		448	462		0.042
5SGX 19L6004	4500	2700	2190	3.0	8.64	0.012		806	769		0.021
	4500	1900	3120	3.7	8.64	0.012		806	832		0.021

Table 2: Ratings and characteristics of the 4.5 kV GCTs.

List of Parameters:

V_{DRM}: [V] maximum forward blocking voltage

$V_{dc\text{-}link}$: [V] maximum dc-link voltage at 100 FIT (refers to the capability of the device to withstand cosmic radiation at sea-level. 100 FIT ≡ 100 Failures per 10^9 operation hours)

$T_{j:}$ [°C] junction temperature

I_{tgqm}: [A] maximum turn-off current at Vdc-link

V_T: [V] forward voltage drop at I_{tgqm} (GCT part)

E_{off}: [J] turn-off losses at I_{tgqm}

$\theta_{jc,GCT}$: [K/W] thermal resistance from GCT junction to case (diode inactive)

V_F: [V] forward voltage drop at I_{tgqm} (diode part)

di/dt: [A/µs] maximum current commutation velocity of the diode at $V_{dc\text{-}link}$

I_{rr}: [A] diode peak reverse recovery current of at a given di/dt

$\theta_{jc,D}$: [K/W] thermal resistance from diode junction to case (GCT inactive)

Part n°	flange diameter [mm]	silicon diameter [mm]	mounting force [kN]
5SGX 03D6004 / 04D4502	51	38	10
5SGX 06F6004 / 08F4502	76	51	15
5SGX 10H6004 / 14H4502	100	68	20
5SGX 19L6004 / 26L4502	125	91	40

Table 3: Mechanical data of the reverse conducting IGCTs

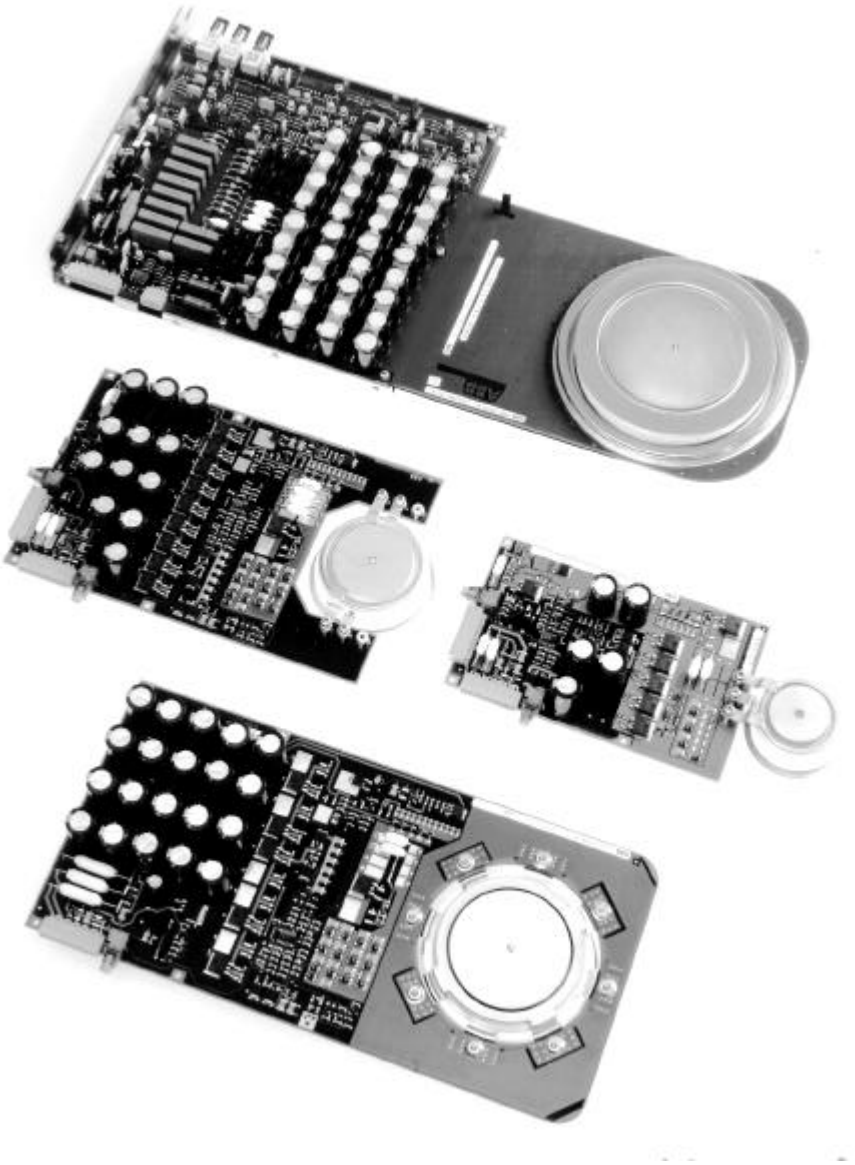

Fig. 5: Photograph of the reverse conducting IGCTs

Additionally a family of discrete diodes has been developed to cope with the needs of system designers for clamp diodes and neutral point clamp diodes. Although these diodes are beyond the scope of this paper, it should be noted that they are optimised to match to their corresponding GCTs.

Characteristics

Switching Behaviour

Fig. 6 shows a possible test set-up for the reverse conducting IGCTs [10]. The inductance Li limits the di_{AC}/dt during GCT turn-on to $V_{dc\text{-}link}/L_i$. In contrast to the IGBT, the turn-on velocity of the GCT cannot be controlled to that extend to allow a snubberless diode turn-off at high voltages without inductive di/dt protection. On the other hand, the combination of di/dt-choke and extremely fast turn-on of the GCT reduces the turn-on losses in the GCT to a close to negligible amount.

To limit the voltage overshoot during turn-off L_i is clamped by the capacitor C_c, the diode D_c and resistor R_c. The clamp design must be such, that the maximum voltage overshoot remains smaller than the maximum blocking voltage. in any cases the clamp capacitor can be much smaller than the dc-link capacitor avoiding the need for costly low-inductance bus-bars.

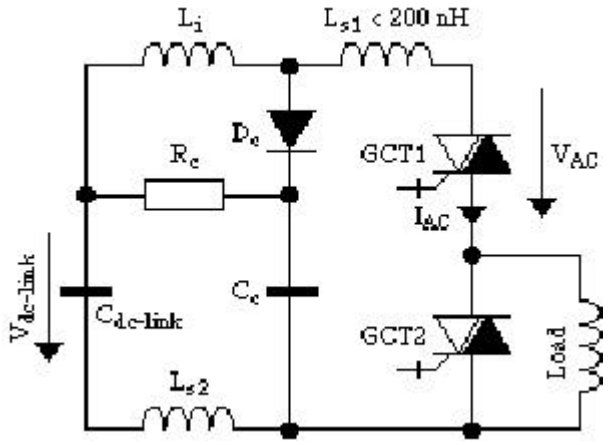

Fig.6: IGCT test set-up

Fig.7 shows typical IGCT switching waveforms [10]. Prior to GCT1 turn-on the freewheel loop was already loaded with a current of 400 A. The current peak immediately following GCT1 turn-on corresponds to the reverse recovery of the diode integrated in GCT2. At a current level of about 520 A GCT1 turns off. The magnification of the turn-off shows, that no decrease of the GCT1 current level can be observed before V_{AC} equal $V_{dc\text{-}link}$ = 3300 V (pure inductive turn-off). The first over-voltage peak results from the stray inductance of the clamp circuit while the second, broader peak is characteristic for the redistribution of the inductive energy stored in the di/dt choke. The short tail period is typical for the buffer layer technology. Note that the total turn-off process from optical triggering of the gate unit until the end of the tail phase last less than 8 µs.

Fig.8. shows turn-off of a monolithically integrated diode of the 5SGX 06F6004 at rated conditions [10]. Note that due to the purely inductive load the diode voltage equals $V_{dc\text{-}link}$ at the reverse recovery peak leading to a high peak switching power. To prevent destruction by dynamic avalanche, the reverse recovery current I_{rr}, must, therefore, be carefully controlled.

As concepts of reverse recovery charge reduction by homogeneous carrier lifetime control would lead to very high on-states and to a snappy diode behaviour, the diode turn-off has been tailored by means of particle irradiation giving the best known compromise between on-state and dynamic behaviour.

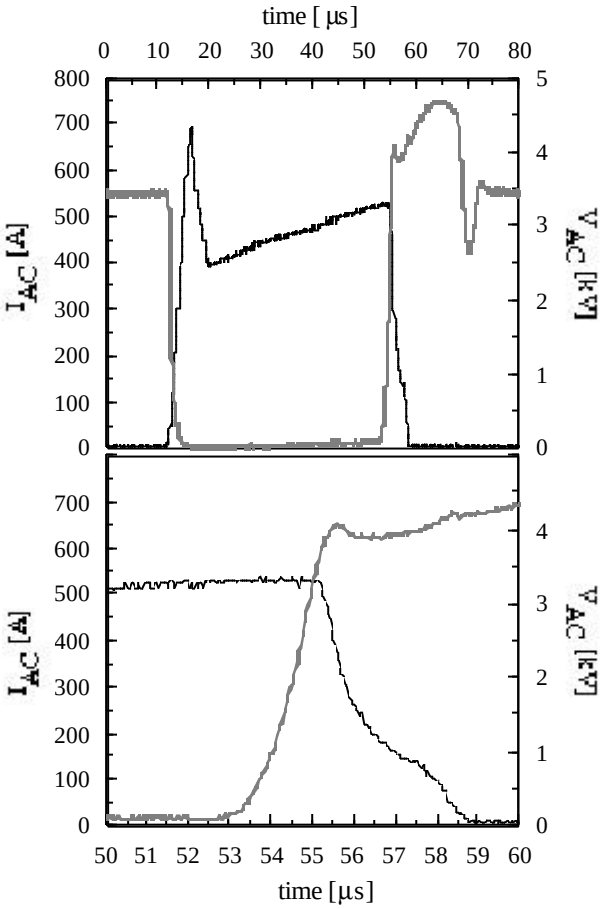

Fig.7: Snubberless operation of the 5SGX 06F6004 at T_j = 115°C

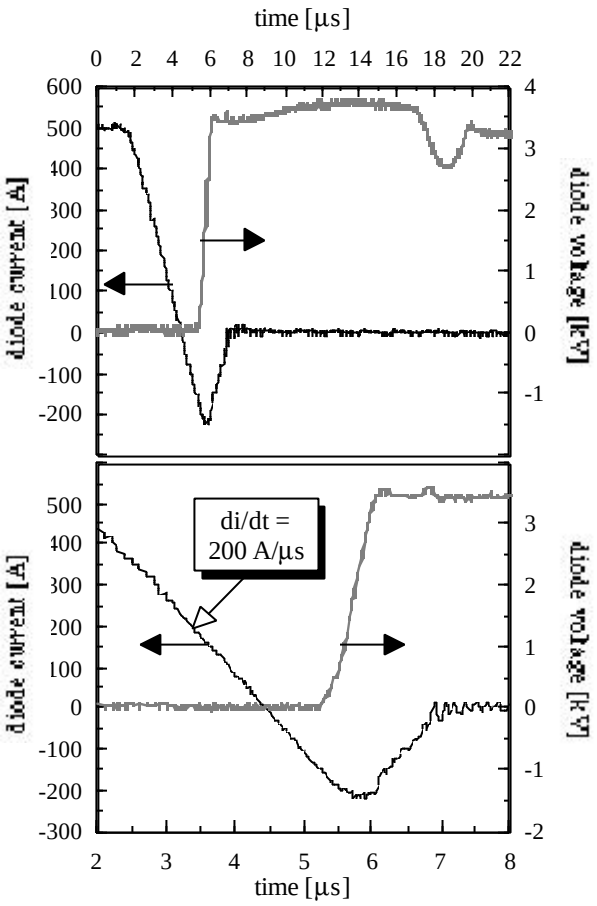

Fig.8°C: Snubberless turn-off of the monolithic freewheeling diode of the 5SGX 06F6004 at T_j = 115

DC-Blocking Capability

As the IGCTs are aimed to operate in an industrial application, it is obvious that they are not supposed to work at a constant DC-voltage. For the GCT design two DC-voltages are of outstanding importance. First, there is the maximum long term DC-voltage at which the GCTs should be capable to operate for a indefinite time at maximum rated conditions. This should correspond to the 10% input over-voltage level of the inverter. ABB Semiconductors' GCTs are designed not to exceed a failure rate of 100 FIT due to ambient cosmic radiation at this voltage. Second, a transient DC-voltage overshoot can occur during braking, worst case at 10% input over-voltage which the IGCTs must sustain for a certain time. Due to a reduced switching activity at these over-voltages the junction temperatures decreases, so that the critical duration to withstand these over-voltages reduces to the time constant of the housing. The maximum transient DC-voltage level of the 5.5 kV IGCTs is 3.9 kV. The IGCTs are designed to withstand this DC-voltage level for more than 10 s at maximum junction temperature. The turn-off capability, however, is reduced to half of the rated turn-off current at 3.3 kV.

High Frequency Pulse Bursts

Traditional GTO thyristors require a fairly long time between two subsequent turn-off operations. This is because its non-uniform turn-off process may lead to non-uniform temperature distributions, which, in turn, may lead to an even more non-uniform turn-off process. Hot spots and thermal runaway can follow. The time between two consecutive turn-off processes is, therefore, governed by the time needed to return to a uniform temperature after turn-off.

The IGCT overcomes this limitation comparable to the IGBT: Due to the turn-off in a transistor mode, no current redistribution occurs, the heat is dissipated homogeneously across the entire junction. The only limit existing for the high frequency operation is the thermal resistance, for continuous operation, or the thermal capacity for high frequency pulse bursts. Fig. 9 shows a 25 kHz, 10-pulse test at 25% duty cycle on the 5SGX 06F6004 [10]. Note that the last pulse occurs at 95% I_{tgqm}. Although, due to the cumulative losses, the permissive junction temperature range is exceeded by far, this transient temperature overshoot is not necessarily critical, as it occurs far from the junction termination. ABB Semiconductors uses this test as a standard final test to judge the homogeneity of switching.

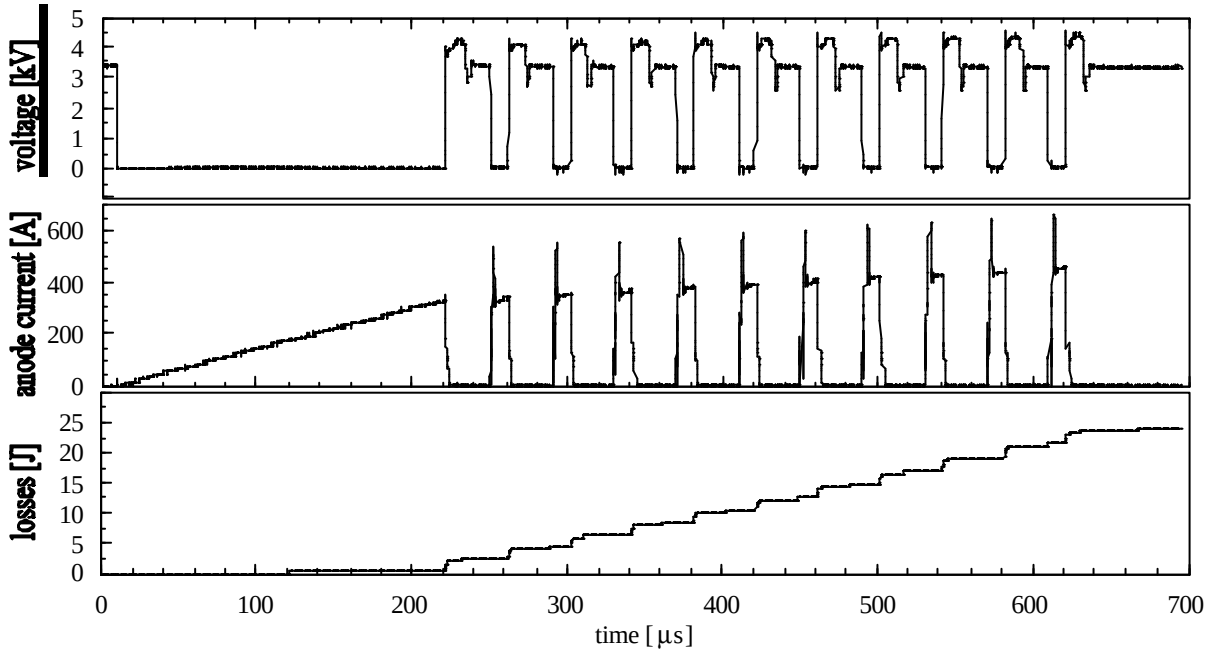

Fig. 9: 25 kHz, 10-pulse test with 5SGX 06F6004. $T_j(t=0) = 80°C$

Inverter Design

The three phase two-level inverter design can be greatly simplified compared to classical GTO circuits [11]. Fig. 10 shows a possible inverter design with IGCTs. The bill of material consists of:

- 6 IGCTs
- 1 di/dt inductor
- 1 clamp diode
- 1 clamp capacitor (high-inductive DC-link)
- 1 clamp resistor
- 1 gate-drive power supply

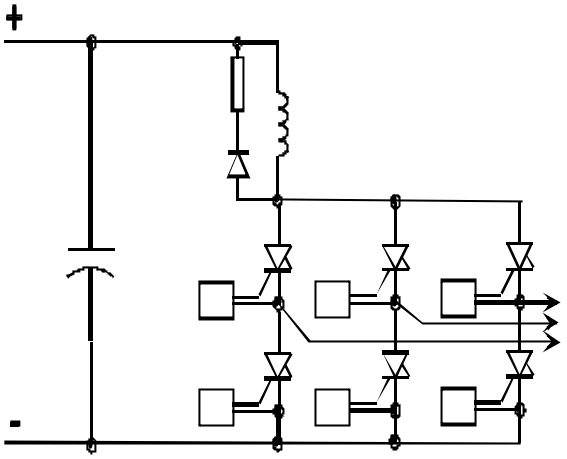

Fig. 10: 3-phase inverter circuit with IGCTs

Estimated maximum inverter ratings are listed in table 4. The calculations consider thermal limits only taking into account a maximum temperature difference of 30 K between semiconductor junction and semiconductor case.

part n°	max. inverter rating at 500Hz [kVA]	max. inverter rating at 1000 Hz [kVA]
5SGX 03D6004 / 04D4502	500	300
5SGX 06F6004 / 08F4502	900	500
5SGX 10H6004 / 14H4502	1400	800
5SGX 19L6004 / 26L4502	3000	1800

Table 4: Possible inverter ratings

Due to the low parts count in combination with the proven field reliability of the GTO technology a high inverter MTBF can be expected. Recent data obtained from a 100 MVA railway intertie indicate, that a MTBF > 45 years or a failure rate less than 2300 FIT can be expected from a 3 MVA 3-phase IGCT inverter. Main FIT rates coming from fibre optic connections and from logic circuits [12].

Conclusions

A complete range of Integrated Gate Commutated Thyristors has been presented in this paper. They offer the possibility to build snubberless Medium Voltage Inverters of up 6 MVA (3-level) without any series or parallel connection of semiconductors. Due to the low parts count and proven reliability of the technology used an extremely high inverter reliability can be expected. With the novel low-loss transparent emitter buffer layer technology usable switching frequencies in the kHz range become feasible. Additionally, a high pulse burst capability allows very flexible control algorithms.

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