SECTION 5

APPLICATION ASPECTS

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APPLICATION ASPECTS

5.1 Introduction

The **G**ate **T**urn-**O**ff thyristor, as its name implies, is a semiconductor device that in operation behaves much like a thyristor, but with the added distinction that it may be turned *off,* as well as *on,* by gate control.

Invented in 1960 [1], the device came into widespread use during the 80's, and has recently undergone dramatic improvements, as will be described later.

5.2 Principle of Operation

The operation and construction of a GTO is similar to that of a thyristor, or *Silicon Controlled Rectifier,* in that it is based on a regeneratively-coupled switching transistor pair. Unlike the SCR however, it has a finely segmented cathode, that causes it to behave like a large number of small thyristors on a common silicon substrate, with common anodes and gates, but individual cathodes.

The GTO's turn-on mechanism is analogous to that of an SCR, but unlike the SCR, turn-off is additionally possible by reversing the gate-current, thereby constricting cathode current towards the centre of each cathode island, where it is ultimately "pinched-off". The ratio of anode current to peak negative gate current is called the "turn-off gain", and current design practice results in turn-off gains of between 3 and 5. Turn-off gain can be increased (the device made easier to turn-off), by reducing the sum of the gains of the constituent pnp & npn transistors (Fig.1). This, however, adversely affects the device's turn-on and conduction performance.

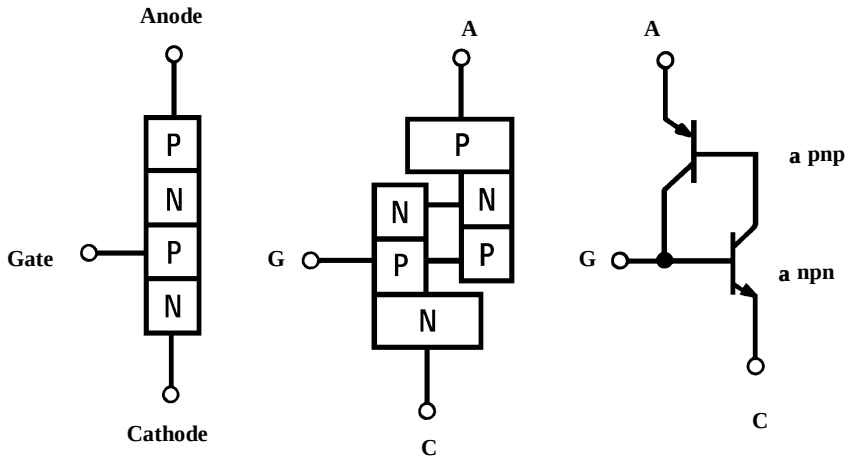


Fig. 1
qqq
Two-transistor
"Regenerative Switch"
Model of a GTO

The four different phases in the switching cycle of a GTO: a) *Turn-On*, b) *On-State*, c) *Turn-Off*, d) *Blocking*, are briefly described below:

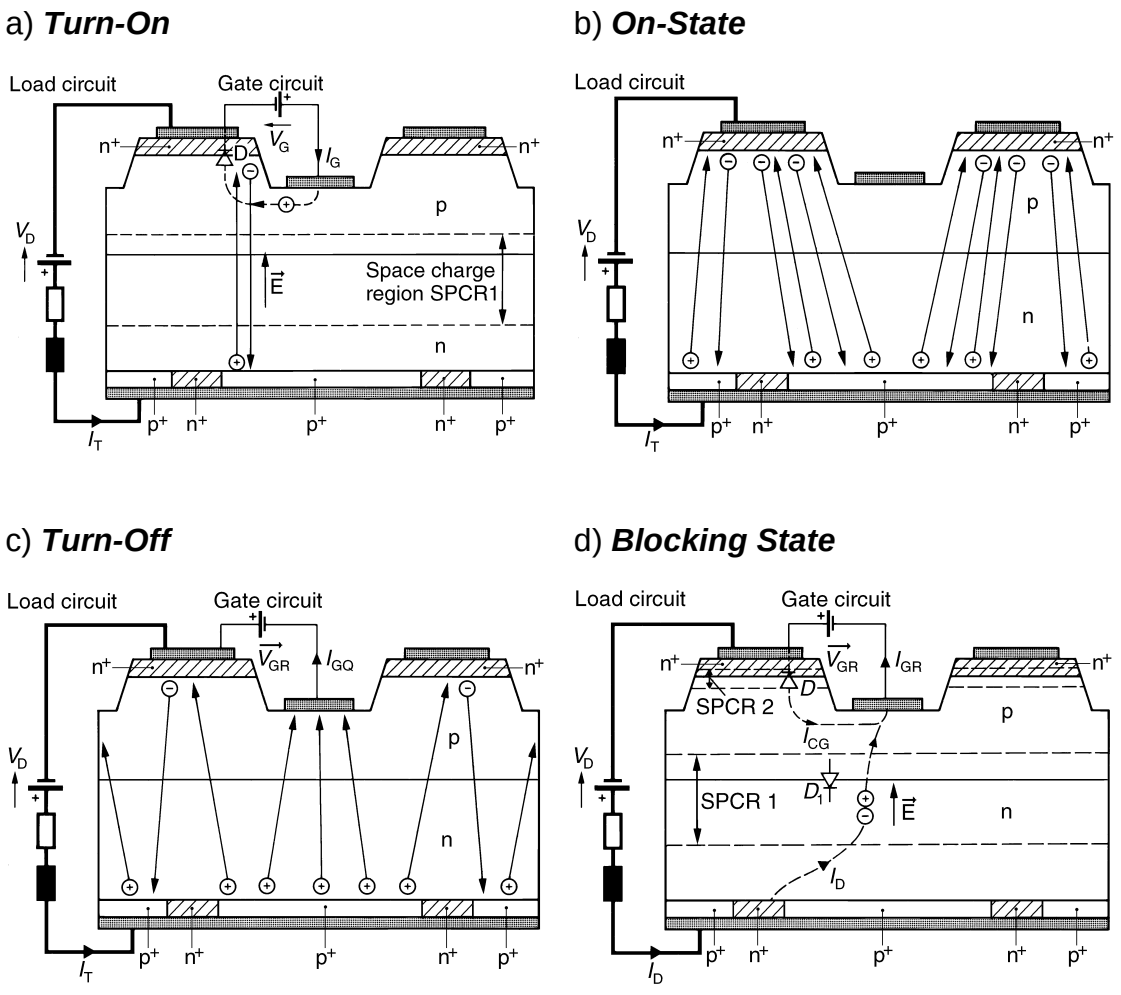


Fig. 2 Switching processes and operating states in the GTO: - electrons + holes

5.2.1 Turn-On (Fig. 2a)

Gate current is injected across the diode junction D to the n^+ layer of the cathode. Because the pn^+ junction is forward biased, the n^+ layer emits electrons into the p base, some of which reach the space charge region SPCR1 of the pn junction which is blocking anode voltage V_D. These electrons are collected by the electric field E and accelerated towards the anode, where they enter the p^+ emitter layer. This polarises the np^+ junction in the forward direction and leads to the emission of holes from the p^+ emitter layer into the n base, some of which also reach the space charge region and are accelerated towards the cathode by the same electric field.
When these holes enter the n^+ emitter layer, they provoke the same effect as the original gate current, i.e. electrons are again emitted from the n^+ layer into the p base, and the process is reinforced. A level of *latching current* is rapidly reached, at which point the process becomes self-sustaining, with the device remaining in conduction, even if the gate current is interrupted - provided the anode current remains above the *holding* level. This regenerative process can be explained in electrical terms by reference to Fig. 1, in which the device gate current is the initial base drive for the npn transistor, whose collector current becomes base drive of the pnp transistor. The pnp collector current in turn becomes the base drive for the npn, and thus, beyond a certain point, external base drive is no longer required.
In the case of a thyristor, a small gate current (about 1 A) is used to initiate the regenerative process, which then “spreads” across a large silicon area, allowing on-state currents of thousands of amps, albeit at a limited rate-of-rise-of-current of a few hundred amps per microsecond. With GTOs, a much larger gate current is required, because many individual thyristors must, in effect, be gated in parallel. If this is done correctly, i.e. with a sufficiently large gate current pulse, all the individual thyristors will ignite simultaneously (there is no spreading effect), and anode current may rise at rates of up to a few thousand amps per microsecond. Depending on wafer diameter and desired anode di/dt, turn-on gate pulses may vary from a few tens to several hundred amps.

5.2.2 On-State (Fig. 2b)

The *regenerative turn-on process* just described, injects a great number of electrons and holes from the emitters into the p and n base layers, which become saturated with charge carriers. The resulting carrier concentrations greatly exceed the doping concentrations of the p and n bases, such that GTOs replicate the low on-state voltage and high surge current capabilities of conventional thyristors.
In Fig. 2.2, the current flow between the emitters is indicated by means of current filaments.

5.2.3 Turn-Off (Fig. 2c)

The turn-off process in the GTO is initiated by a negative gate current. Due to the high conductivity of the p-base, holes arriving from the anode partially flow to the negatively polarised gate contact. During the *storage time*, the current progressively *filaments* towards the middle of the cathode segments, until the filaments are finally "pinched off". At this instant, the anode current falls rapidly, and both the pn+ and pn junctions are again able to sustain voltage.
The filamentation of current, towards the cathode centres, reduces the active silicon area during the critical turn-off phase. This would be a minor limitation, were it not compounded by the filamentating current tending to commutate to those cathode areas remotely located from the extinguishing gate current. This re-distribution of cathode current continues during the storage time (tens of microseconds), and culminates with a rising anode voltage and a falling cathode current. It is this phase which requires the presence of a snubber (i.e. a capacitance) across the device, to limit the re-applied dv/dt to between 500 and 1000 V/µs. Fig. 3 illustrates this short phase in which both anode voltage and cathode current co-exist, with the danger of re-triggering that this represents.

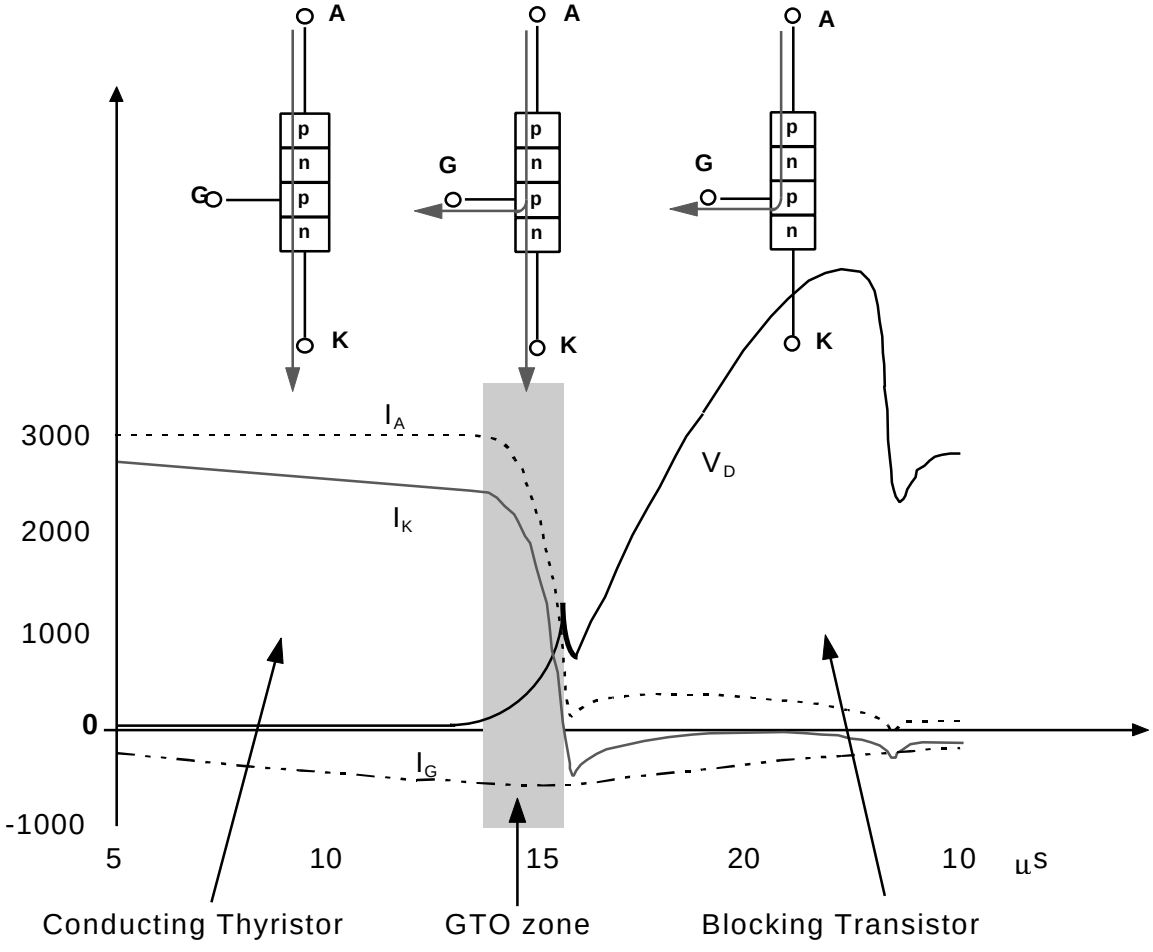


Fig. 3 Conduction and Conventional Turn-off of a GTO

The p^+ emitter layer of a conventional asymmetric GTO (see also Section 2 “Product Design”) contains n^+ islands, or *anode shorts,* with a pattern similar to the segments on the cathode side. These act to limit the gain of the anode emitter, which facilitates the turn-off process, and also provide a low impedance path for charge carriers during turn-off, thus reducing turn-off losses. Section 2 also describes *the Transparent Emitter,* which requires no such shorts. Here, the emitter is thin, weakly doped, and of inherently low gain; it thus appears “transparent” to charge carriers during turn off. This transparence can be likened to a pattern of infinitely distributed shorts - more effective than localised finite shorts.

5.2.4 Blocking State (Fig. 2d)

During the blocking state, the GTO is almost free of mobile charge carriers. The blocking voltage V_D, applied by the external electrical circuit, creates a space charge region SPCR1, while the negative gate voltage, $V_{GR,}$ polarises diode D in the reverse direction, leading to space charge region SPCR2. The reverse blocking capability of this pn+ diode is limited to about 20 V. Under these conditions, the GTO behaves totally as a pnp transistor, since the reverse biased gate-cathode region prohibits npn transistor action. Provided the biasing supply is of negligible impedance, the GTO has a virtually unlimited dv/dt capability.
From the above, it can be seen that a conventionally driven GTO acts like a thyristor in 3 of the 4 operating modes.

5.3 Gate Drive

The GTO gate drive has to fulfil the four following functions:

1. Turn the GTO on by means of a high current pulse (I_{GM})
2. Maintain conduction through provision of a continuous gate pulse during the on-state (I_G also known as the “back-porch current”)
3. Turn the GTO off with a high negative gate current pulse (I_{GQ})
4. Reinforce the blocking capability of the off-state device, by negative gate voltage or, at least, by a low impedance resistor.

Careful gate-unit design is an indispensable prerequisite for reliable circuit operation. For this reason, the above mentioned functions are discussed below in further detail with reference to Fig. 4.

5.3.1 Turn-On

The initial gate-current pulse I_{GM} initiates switching along the gate periphery. Recommended values of di_G/dt and I_{GM} can be taken from the data sheet, where the influence of I_{GM} on the turn-on energy and switching times can also be found. A rough guide to the required value of I_{GM} is that it be at least 6 times the device’s I_{GT} value, at the temperature of interest.

For a GTO with a 3 A I_{GT} at 25°C, I_{GM} should be 20 A at 25 °C, or 60 A at -40°C, for the values of anode voltage and di/dt cited on the data sheet (50 % V_{DRM} and 300 to 500 A/µs). The rate of rise of this current pulse is also important, and it should be at least 5% of the anode di/dt, with a duration at least equal to the sum of the delay and rise times ($t_d + t_r = t_{gt}$), also to found on the data sheet.

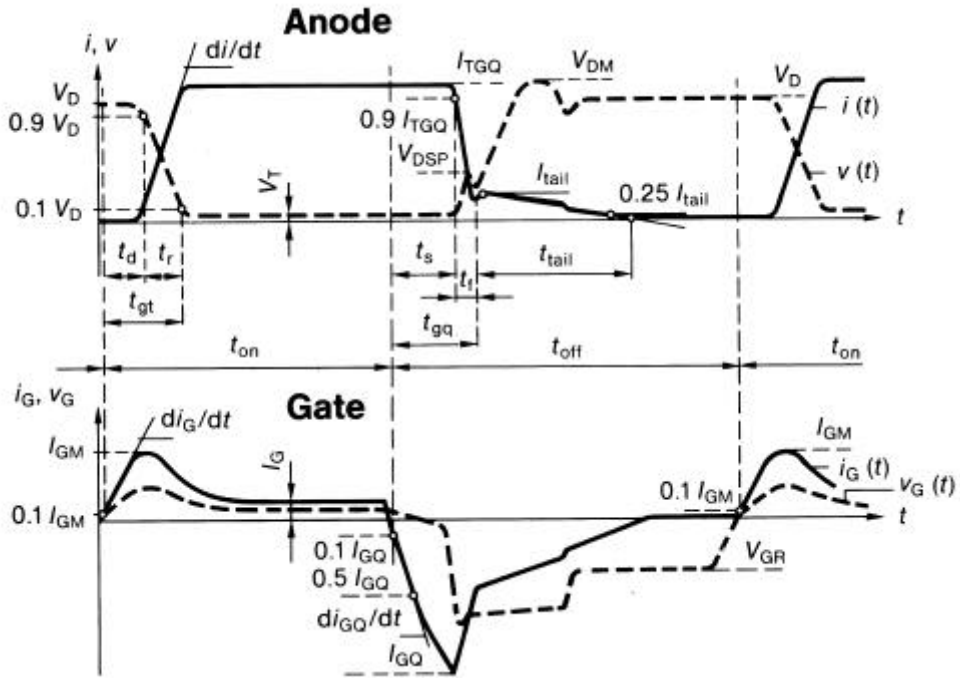


Fig. 4 Current and Voltage Waveforms and Parameter Definitions for GTOs

Since device turn-on is affected by many parameters (anode voltage, snubber discharge, repetition-frequency, temperature, pulse-duration etc.), a qualitative assessment of adequate turn-on can be obtained by observing the anode voltage collapse. A pronounced increase of anode voltage during anode current rise, such as can be seen later in Fig. 10 (“soft turn-on”), should be avoided.
It is obvious that GTOs require much more gate current than conventional thyristors due to the following:

- The initial plasma spreading front (i.e. the contact line between gate and cathode area) is very long due to dense segmentation of the GTO.
- GTOs have no amplifying gate, thus the whole current at the turn-on front must be delivered by the gate unit alone.
- Due to the required turn-off capability, the p-base conductivity is high, and anode emitter efficiency is low, which hampers the turn-on process.

On the other hand, the dense segmentation is beneficial at turn-on: the entire cathode area is ignited within a few microseconds, in contrast with thyristors, which may take several milliseconds to fully propagate. Such long propagation times produce higher turn-on losses, and restrict allowable anode di/dt. Furthermore, GTO-like structures are eminently suitable for use in high-current pulsed-switching applications. As will be seen in Chapter 4, very fast turn-on can be achieved (> 20 kV/μs) if the device is triggered with very high gate currents.

5.3.2 Conduction

In the on-state, the GTO is a thyristor. In many applications, especially when the load is a motor, the load current may momentarily fall to a low value, then rise again. Under such conditions, a GTO without gate current may partially unlatch, that is, the current density may be insufficient to maintain the entire cathode area in a latched thyristor mode. This is, in itself, harmless but the consequential undefined conducting area results in an equally undefinable di/dt capability. Should the load current rise rapidly, current crowding could result, possibly provoking an apparent di/dt failure.
This can be circumvented by supplying a continuous gate current (also known as the “back-porch” current), preferably at least 20% greater than the gate trigger current I_{GT}, in order to keep all segments in the conducting state.
This continuous gate current (back-porch) is all the more important when the load current becomes negative, and load current flows through the free-wheel diode. In this condition, the GTO returns to its off-state, and any gate current tends to be diverted away from the cathode towards the anode. The device may then be unable to reabsorb the load current, when this latter becomes positive, and allows the back-porch current to return to the cathode. With inadequate gate current to ensure re-triggering, and no negative gate voltage to ensure blocking, the device could spuriously and destructively re-trigger at some anode voltage below its normal rating. Conventional GTOs, with a turn-off current of 3000 A, require a continuous gate current of over 10 A at -40°C (given in the data-sheet as a function of the junction temperature). Because this value is highly temperature dependent, it is useful to modulate it as a function of temperature.

5.3.3 Turn-Off

The GTO turns off when gate current is reversed, with an amplitude of 20 to 30% of anode current. The process has been described in Section 2. Reference to Fig. 3 shows that there is a critical period, during which anode voltage is sustained while cathode current is still flowing. The duration of this period is dependent on the rate-of-rise of negative gate current. If di_{gn}/dt is low, not only is the period of high dissipation prolonged, but more importantly, a longer time is available for current to redistribute through the numerous GTO islands, with worsened current inhomogeneity.

As a consequence, a design goal for gate units should be to maximise di_{gn}/dt, which minimises storage time and increases the safe-operating area (minimises snubber requirements).

5.3.4 Blocking State

In the blocking or “off-state”, the preferred gate condition is one of negative bias greater than 2 V. However, any voltage up to the rated gate-cathode value is suitable, while the source impedance should be as low as possible. Under these conditions, the device has virtually no dv/dt limitation, as it behaves as a simple low gain bipolar transistor with open base.
Under certain conditions, it may be necessary for the GTO to block forward voltage capability without an energised gate unit, as during start-up or fault conditions). In these cases, a resistor permanently connected between gate and cathode may suffice, the ohmic value of which (2 to 20 Ω) depends on the device, its temperature, and the required voltage. When such a resistor is used, instead of a low impedance voltage source to bias the gate-cathode junction, the GTO behaves like a thyristor; as such it again has dv/dt limitations. See Section 3 for more details.

Summarising the basic requirements of a drive unit:

- high I_{GM} and dig/dt for homogeneous turn-on
- back-porch current > 1.2 I_{GT}
- high di_{gn}/dt for *low* turn-off gain and minimised filamentation
- forward gate-current or reverse-gate voltage at all times.

5.3.5 Gate Drive Circuit

There are different approaches to GTO gate drive design. In the following, a gate drive is described that is suitable for both industrial and traction applications.
In the block diagram of Fig. 5, it is assumed that there is a potential difference of a few kilovolts between the master control electronics and the individual gate units. The DC supply voltage, delivered from a common power supply, is converted to high frequency AC by means of inverter block A, transferred across the isolation barrier by transformer B, where it is rectified and regulated by block C to provide voltage for the gate unit’s control circuit.
The control signals from the master control are transmitted to the logic Block F, via fibre-optic cables and photo transistors (Block E). Block F converts these signals into gate pulses for the transistors in Block D. According to the application-specific requirements, the control logic may also supervise GTO conduction by monitoring the gate-cathode voltage, as well as gate unit supply voltage levels. Any faults are relayed via fibre-optics back to the master control. A possible circuit for the output stage of the gate unit (Block D) is shown in Fig. 6. C_1, R_1, C_2, R_2 and T_1 form and transmit positive gate current. T_2 and C_3 constitute the turn-off channel, and provide negative gate voltage during the GTO’s blocking period.

R_1 determines amplitude of the continuous gate current, whereas R_2 and C_2 shape the initial gate pulse (I_{GM}). R_3 guarantees minimum blocking capability for the GTO in case the gate unit power supply fails. T_2 consists of several transistors in parallel, depending on the required maximum negative gate current $I_{GQM.}$

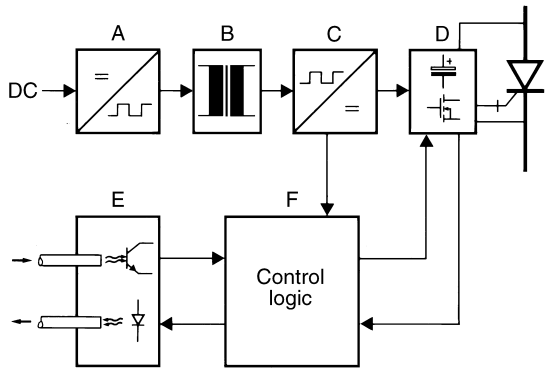


Fig. 5 Block Diagram of Typical GTO Gate Unit

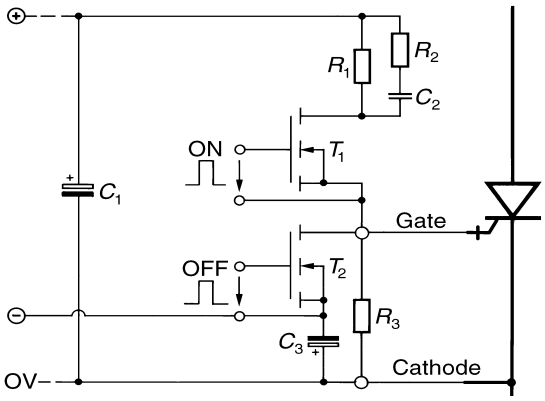


Fig. 6 Possible Circuit for Output Stage D of Fig. 5

5.4 Integrated Gate-Commutated Thyristors

The continuous search for higher performance, higher reliability semiconductor devices, has led to a dichotomy in recent times over whether the device of choice should have essentially a *transistor,* or a *thyristor* structure. Thyristors are generally preferred for their low conduction losses, and transistors for their rugged turn-off capabilities. Numerous structures have been proposed, divided along these lines. Some strive to have the best of both worlds, exploiting the rugged on-state performance of thyristors, while reverting to a transistor like behaviour prior to the critical turn-off phase:

THYRISTORS	**TRANSISTORS**
GTO (Gate Turn-Off Thyristor)	BIPOLAR TRANSISTOR
MCT (Mos-Controlled Thyristor)	DARLINGTON TRANSISTOR
FCT (Field-Controlled Thyristor)	MOSFET
MTO (Mos Turn-Off Thyristor)	IGBT (Insulated Gate Bipolar Transistor)
EST (Emitter-Switched Thyristor)	
IGTT (Insulated Gate Turn-off Thyristor)	
IGT (Insulated Gate Thyristor)	
GCT (Gate-Commutated Thyristor)	
IGCT (Integrated Gate-Commutated Thyristor)	

Until recently, the only serious contenders for high power applications were the GTO, with its cumbersome snubbers, and the IGBT, with its inherently high losses. Recent developments, however, have led to a device that truly combines the best of thyristor and transistor characteristics, while fulfilling the additional requirements of manufacturabilty and high reliability. The **G**ate-**C**ommutated **T**hyristor is a semiconductor based on the GTO structure, whose gate circuit is of such low inductance that the cathode emitter can be turned-off quasi instantaneously, thereby converting the device to a bipolar transistor at turn-off, and eliminating the need for a snubber [2].

5.4.1 Turn-off

Turn-off will be described first, in that the turn-off phase is the most important aspect of the GCT's performance. Because the physical process has been described in some detail in Section 2 , only an overview is required here.
Reference to Fig. 3 and Section 5.2 serves to remind us of the GTO's principal weakness, which is the short duration "GTO turn-off zone", during which both anode voltage and cathode current co-exist. In this zone, the risk of regenerative triggering always hovers, and re-applied dv/dt must be limited. It has been shown [3] that there exists a critical rate-of-change-of-gate-current, above which this narrow GTO zone no longer exits. Under such conditions, the GTO is best described as a "**G**ate-**C**ommutated **T**hyristor " in which the pnp transistor turns off uniformly with an open n-base, as would a three-terminal Darlington or an IGBT. This preferred mode of operation, known as "hard turn-off, requires no snubber, as the device is a simple transistor structure with virtually no dv/dt limitations. (See also Section 2.)

Fig. 7 shows the turn-off of a 3 kA GCT based on the ABB Semiconductors' type 5SGT 30J4502 Transparent Emitter GTO. Since no snubber is used, the resulting anode dv/dt is a characteristic of the device. It can be controlled at the wafer production stage by adjusting the anode profiles. As with transistor turn-off, slowing the rate-of-rise of anode voltage increases turn-off losses. *Unlike* transistors, this rate-of-rise is not gate controlled. The GCT can be synthesised from a GTO and a high voltage, low inductance gate driver [3]. However, to enable the special unity gain operating conditions to be fulfilled economically, GCTs are normally encapsulated in specially constructed, low inductance housings. ABB Semiconductors also supplies these devices integrated with their gate-drivers, when they are then known as IGCTs. An example of a GCT housing is shown in Fig. 8. Such a housing can accommodate wafers of various voltage and current ratings, as well as unidirectional and reverse conducting devices. See also "Device types".

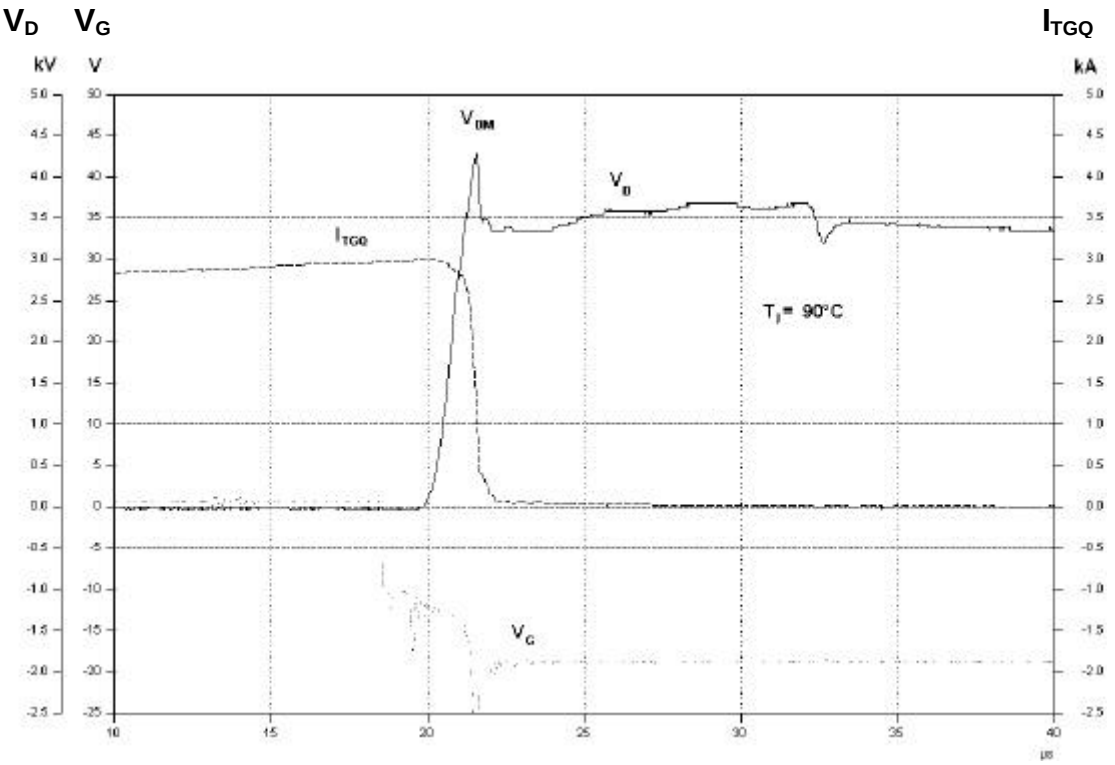


Fig. 7 Snubberless Turn-off of a 3 kA/4.5 kV GCT

Fig. 8 Example of a GCT Housing and Wafers

The critical-rate-of-rise of negative gate current referred to above is 3000 A/µs, which corresponds to diverting the maximum instantaneous anode current out of the gate in less than one microsecond. Thus, the complete gate circuit must feature very low inductance (< 7 nH), and be able to sink the entire anode current for about 1 µs, from a 20 volt supply. It can be seen from Fig. 7 that gate voltage develops about 2 µs prior to any change occurring in the anode current. At the instant gate voltage appears, the cathode emitter is out of action, and the GCT is transformed into a transistor. The resulting turn-off waveform of is clearly that of a transistor.

Fig. 9 shows a 4 kA/4.5 kV Integrated Gate-Commutated Thyristor switch comprising a GCT as per Fig. 8 and a corresponding low inductance drive unit.

In the case of GTOs, the allowable turn-off current is primarily a function of the re-applied dv/dt (snubber capacitance). For snubberless IGCTs, it is the re-applied *voltage* which determines turn-off capability, and hence the maximum turn-off current is given by:

$$I_{tgq} = A_a * k_p \text{ kW}/V_{dm}$$

where V_{dm} is the reapplied voltage, A_a is the anode area in cm^2, and k_p is the allowable power density, typically 200 to 250 kW/cm^2.
Further details on I_{tgq} ratings can be found in Section 3.

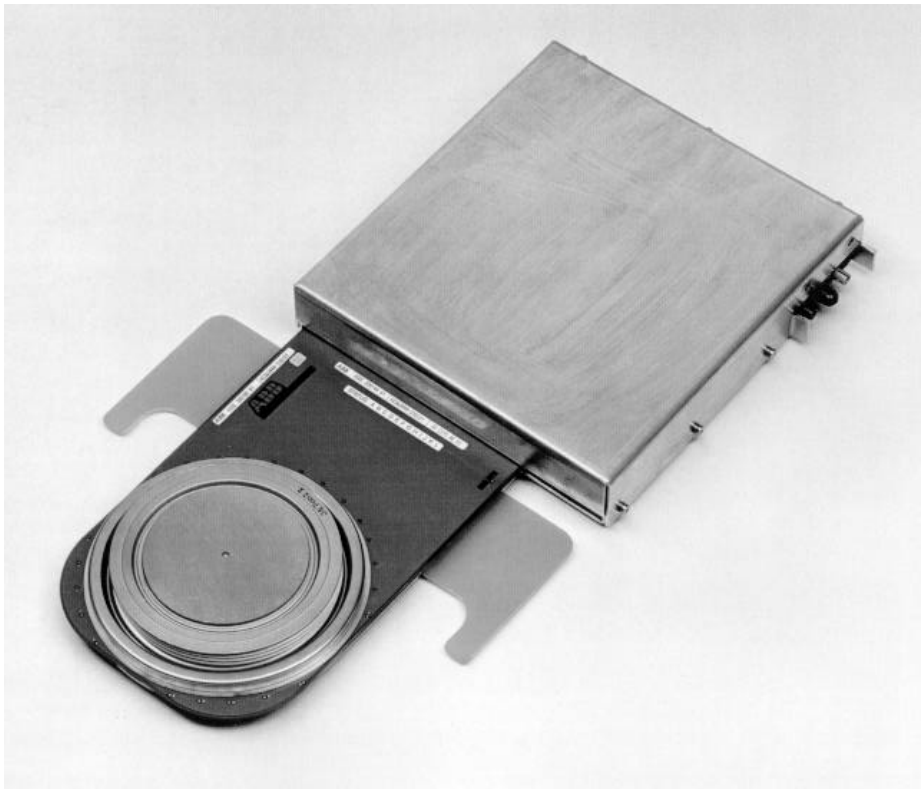


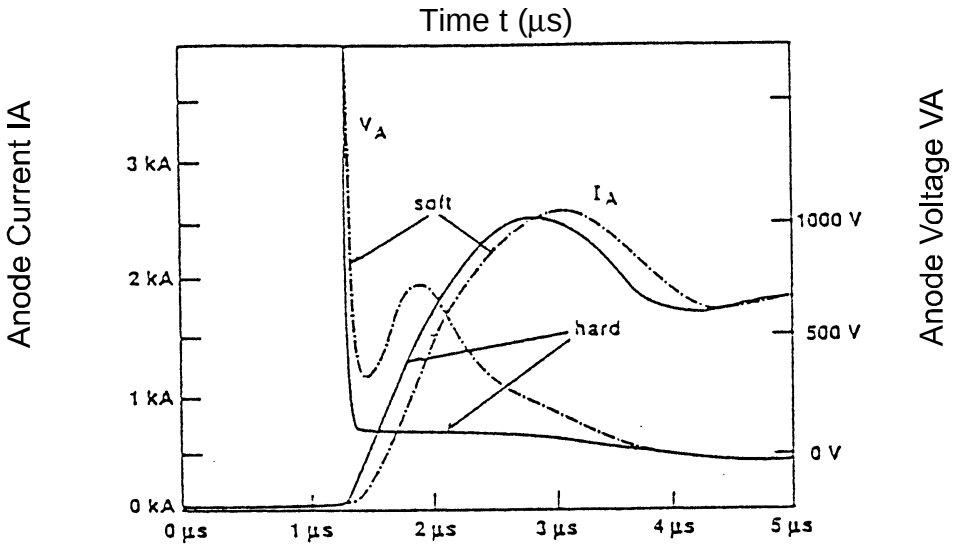
Fig. 9 Gate-Commutated Thyristor Switch Assembly for 4.5 k>V/4 kA

5.4.2 Turn-On

The GCT can be turned on like a GTO - with a relatively low gate current (tens of amps) - but is then subject to the same di/dt limitations as its progenitor. It can, however, also be turned on like a transistor, when the npn transistor is driven so hard (by a high amplitude external base-drive), that regenerative switching occurs only after uniform saturation of the “npn cathodes”. It has been shown [3] that transistor turn on of a GCT, also known as “hard turn-on”, allows a ten-fold increase in turn-on di/dt, or a ten-fold reduction of turn-on losses.

Fig. 10 illustrates turn-on of a 3 kA/4.5 kV GTO at 3 kA/µs. The anode voltage trace resulting from the 500 A gate pulse, designated “soft” turn-on, shows that the voltage first collapses, then rises again with the fast rising anode current, before falling once more to the on-state value. This is a common phenomenon in thyristors, and is commonplace at high anode di/dt values. It indicates that current density is increasing during the regenerative switching phase. In the case of GTOs, because this phase is dependent on the gains of two transistors, which is in turn depend on their individual collector currents and temperatures, a potentially unstable situation exists, which could result in inhomogenious turn-on of the individual cathode islands. With the “soft” drive of Fig. 10, it must be supposed that not all the 2000 individual thyristor elements are regenerative switching at the same rate, and that inhomogenious turn-on may be the result: turn-on power losses will be higher, but worse, their distribution across the silicon wafer will be unknown.

By comparison, the “hard” turn-on wave-form demonstrates a monotonically decreasing anode voltage, despite the fast rising anode current. Here, the turn-on mode is dominated by turn-on of the npn transistor, which pulls down the anode voltage at some 20 kV/µs, and saturates uniformly. Regenerative action is delayed by the rapid disappearance of the space charge region, and occurs at a low anode voltage (<200 V). Despite the fast rising anode current, anode voltage reduces continuously over a 3 to 4 µs period, as the device converts from an npn transistor to a pnpn thyristor. In the hard-driven on-mode, homogeneous transistor turn-on occurs, with no current crowding or “hot spots”, and turn-on losses are reduced by an order of magnitude.



Turn-on measurements

@ I_{gmax} = 1000 A (hard)

@ I_{gmax} = 500 A (soft)

Fig. 10 “Hard” turn-on compared with “soft” turn-on, in a 3 kA/4.5 kV GTO

5.4.3 Conduction

This phases is identical to that of a GTO, in that the conducting state of the GCT is characterised by the very low losses of a thyristor.

5.4.4 Blocking

In the off-state, the GCT behaves like an open base transistor. In this respect, it differs slightly from a GTO, in that it is virtually impossible for the device to be spuriously gated by ambient electrical noise or reapplied dv/dt, as the coupling between gate unit and device is of negligible impedance.

5.4.5 Transparent Emitters

Transparent emitter GTOs are described in Section 2. This technology can be exploited to great advantage in IGCTs for the reasons given below. All ABB Semiconductors’ GCTs have transparent emitters.

Conduction Losses

Reference to Table I shows that TGTO technology yields a 30 % or more reduction in the normal on-state losses.

Turn-off Losses

Transparent Emitter Technology also reduces turn-off losses by about 30 %. Furthermore, from the instant that the cathode is commutated off, anode current will flow out of the gate and contribute to the gate power requirements. TET is therefore helpful in reducing the off-section of the gate driver.

Back-Porch Current

As has already been explained, it is necessary to maintain continuous gate current (see paragraph 3.2) when a free-wheeling diode conducts. The magnitude of this current is proportional to I_{gt}, at the temperature of interest. Transparent Emitter GCTs, unlike conventional GTOs, require no anode shorts, and therefore have very low trigger, and correspondingly back-porch, current requirements. This minimises on-gate power needs. Table I summarises the different values of I_{gt} for ABB Semiconductors' GTOs and GCTs.

Table I - COMPARISON OF GTO, TGTO AND HD-TGTO 4.5 kV, 85 mm

3 kA, 4.5 kV,125°C unless otherwise stated	GTO 5SGA 30J4502	TGTO 5SGT 30J4502	GCT 5SGY 30J4502*
	Specification Limit Values		
on-state voltage V_{tm}	4 V	2.1 V	2.1 V
on-state loss at 1 kA dc	2600 W	1500 W	1500 W
turn-off energy E_{off}	12 Ws at 6 µF	6 Ws at 6 µF	10 Ws at 0 µF
snubber requirements C_s	6 µF/300 nH	6 µF/100 nH	0 µF
rms current I_{rms}, at T_c = 85°C	1460 A	1800 A	1800 A
peak turn-off current I_{tgq}	3 kA at 6 µF	3 kA at 6 µF	3 kA snubberless 6 kA at 6 µF
gate drive power at f_t = 500Hz, 1150A_{RMS} (3)	80 W	30 W	15 W
max. turn-off dv/dt	1000 V/µs (1)	1000 V/µs (1)	3000 V/µs (2)
I_{gt} at 25 °C	3 A	0.3 A	0.3 A
gate stored charge Q_{gq}	8000 µC	8000 µC	2000 µC
typical back-porch at -40 °C	12 A	2 A	2 A

* Device not currently in production: see 5SGY 35L4502 in "Data Sheets" section.

(1) rating (2) characteristic (3) PWM operation in H-bridge, output frequency f = 50 Hz, switching frequency f_t = 500Hz, phase current I_{phase} = 1150A_{RMS}.

Note 1:

The gate turn-off charge of an IGCT is only 30 % that of a conventional GTO (defined up to I_{GQ_max}). Coupled with a 60 % reduction of tail current (after $I_{GQ\ max}$) and a factor 10 reduction of on-gate current, in the case of TGTOs, this leads to the 50% reduction in gate-drive power requirements.

Note 2:

With snubber, the turn-off losses of a TGTO are half those of a conventional GTO. A snubberless IGCT has approximately the same losses as a standard snubbered GTO.

Table I illustrates the significant differences between conventionally driven GTOs and GCTs.

5.4.7 Summary

Whereas the GTO is a thyristor in all four of its operating phases: *turn-on*, *conduction*, *turn-off* and even *blocking* (if the gate-circuit impedance is not negligible), the GCT is a thyristor ***only in the conducting state***. This, combined with emitter transparency and buffer layers, as described in Section 2, offers the lowest possible static and dynamic losses, and the highest switching powers of any currently available semiconductor. Thanks to its monolithic structure, it can be pressure assembled in hermetic housings, making it suitable for high reliability applications, where low failure rates and low wear-out are required. It achieves the long sought-after goal of combining the best features of thyristor and transistor structures, and leads to the type of circuit simplification depicted in Fig. 11, which compares the complex Undeland inverter phase-leg with a much simpler reverse conducting GCT equivalent.

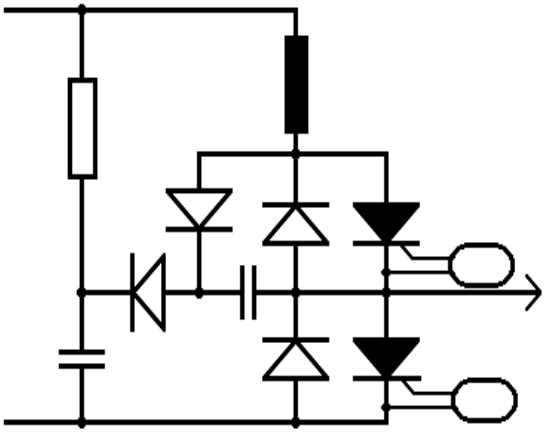


Fig. 11a Undeland Inverter GTO Phase-Leg

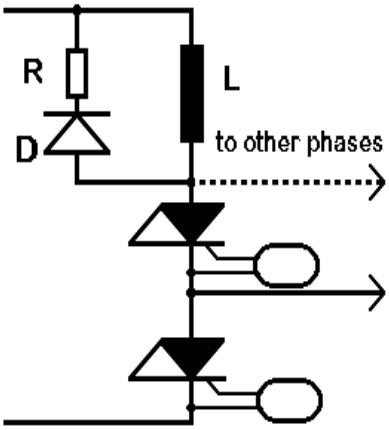


Fig. 11b Reverse Conducting GCT Phase-Leg

Because turn-on di/dt cannot be controlled by the gate, a turn-on di/dt limitation element is still needed to prevent excessive *turn-off* di/dt in the free-wheel diodes. This is because the GCT transistor turn-on mode is very short, whereafter it becomes a conducting thyristor. In many transistor inverters, free wheel diode commutation is controlled by slow turn-on of the transistors, thereby increasing losses in the active switches. With GCTs, this is done externally (L) and the resulting losses are therefore external too (R).

5.5 Device Construction

The construction of a GTO is similar to that of most press-pack semiconductors, and is illustrated in Fig. 12. The press-pack is particularly suited to high power applications because, as its name implies, the various device parts are pressed together, not brazed or soldered, thus allowing the constituent materials - from silicon wafer to copper current conductors - to slide freely over each other during decades of fatigue-free thermal cycling.

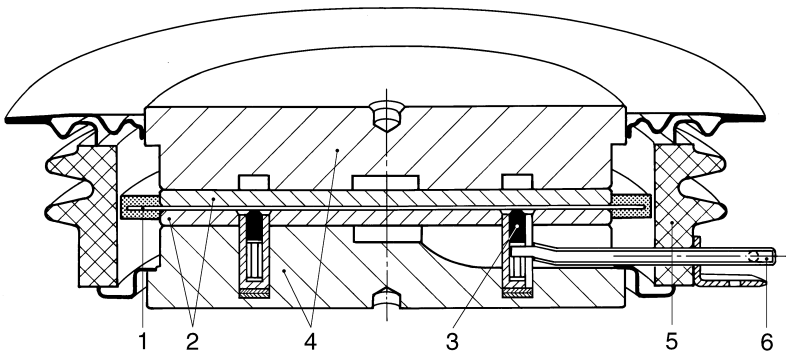


Fig. 12 Construction of a press-pack GTO

Legend: 1 Silicon wafer
2 molybdenum strain buffers
3 Gate electrode
4 Copper pole-pieces
5 Ceramic ring
6 Gate connection

The gate electrode is recessed in the copper pole-piece on the cathode side, and electrically isolated. For small wafer diameters, a central gate contact is sufficient, whereas for GTOs with high turn-off currents above about 2000 A, the gate electrode is, in most cases, annular thus halving the distance between the gate contact-to-wafer and the most remote cathode fingers. Fig. 13 depicts various wafer designs.

Fig. 13

Cathode-side view of various GTO wafers

The contact pressure for the gate is produced by a spring assembly inside the housing, and is thus independent of external mounting force.

ABB Semiconductors uses its patented **F**ree **F**loating **S**ilicon **T**echnology (FFST) for most high power semiconductors, including GTOs. See Sections 2 and 4 for further details on the Design and Reliability of FFST.

As with most ceramic housings, the package is back-filled with nitrogen, then hermetically sealed to ensure long-term stability of both the blocking junction and contact interfaces.

5.6 Areas of Application

Forced Commutated Inverters and Choppers require the use of switches which can be turned off as well as on. The GTO was invented in 1960, but due to manufacturing difficulties it was the fast thyristor that held sway in the '60s and '70s, though this could not be turned off by gate control. In a thyristor inverter, the entire anode current has to be commutated away from the device under full anode voltage. The '80s saw a substantial improvement in the power capability of transistor devices, such as bipolar transistors and Darlingtons, where only a small fraction of the collector current is used for control, and this at base-voltage levels. The IGBT also made its appearance in the early '80s, allowing MOSFET-like control from fundamentally low-cost voltage-sources. Nevertheless, these transistor based devices were never able to satisfy the higher power needs of industrial motor drives and transportation, and the GTO made a re-appearance during this decade. Offering the high current and voltage attractions of thyristors, with control currents of 20 % anode current, and at gate voltage levels of only 20 V. However, a large snubber remained obligatory - an evolutionary link to the fast thyristor commutation circuits of the past, and to the fundamental need to limit reapplied dv/dt across a thyristor structure.
The '90s saw continued improvements in GTO devices, and marked improvements in IGBTs, as consensus grew in the power electronics industry that the ideal semiconductor should operate *without* snubbers, for circuit simplicity (cost and reliability).

5.6.1 New Technology

A major improvement in GTO technology occurred in 1994, with the development of the GCT (already described), in which fast unity-gain turn-off (*gate* commutation of the *anode* current) allows snubberless operation by suppressing the thyristor structure in all operating modes but conduction. This, coupled with ABB's advanced Transparent Emitter Technology (TET) introduced in 1995, has resulted in a snubberless switch for high power applications, permitting simple inverter designs with half the losses of alternative technologies. Reverse conducting devices - of optimal design thanks to TET - further enhance circuit simplicity. An additional advantage of this turn-off mode is that storage time is reduced, from the usual 25 μs to about 1 μs. This considerably enhances turn-off response, especially under fault conditions, but more importantly makes it possible to series-connect components without prior parametric selection, and without active gate control of storage times or anode voltages.
Not only are the needs of industrial and traction drives satisfactorily addressed by these new devices, but hitherto impractical circuit topologies --- needing series devices for, say, 100 MW inverters in Utility and Railway Interties ---- are now a reality [4].

Furthermore, the GCT offers possibilities in resonant circuits, because of its ability to satisfy the demanding requirements of such industries as Induction Heating, namely:-

- high voltage (< 6 kV)
- high dv/dt (> 3 kV/µs)
- high peak current (>5 kA)
- high di/dt (≈ 3 kA/µs)
- zero turn-off times (0 µS)
- high frequencies (> 20 kHz)

Present and emerging applications for GCTs include:

- Medium Voltage Drives (line voltages up to 6.9 kV rms)
- Railway Power Supply Frequency Changers
- Utility Interties
- STATCOMs (static compensators for leading and lagging power factor control)
- UPFCs (unified power flow controllers for utilities)
- Utility Active Filters
- Industrial VAR Compensators
- Deep Sea Pump Drives
- Marine Drives/All Electric Ships
- Transformerless Traction Supplies
- Locomotive Drives
- Induction Heating Resonant Inverters
- Static Breakers

5.6.2 Voltage Source Inverters

Fig. 14 shows the basic circuit of a voltage source inverter, consisting of six GTOs - for active power control to the motor - each with an anti-parallel free-wheel diode - for returning reactive and braking power from the motor.

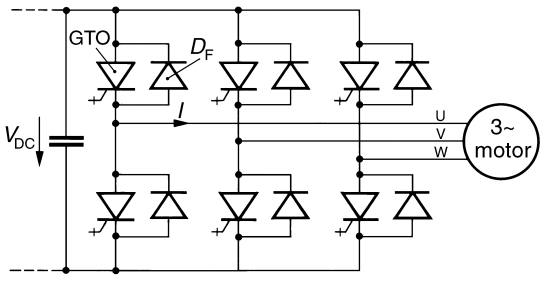


Fig. 14

Basic Circuit of a 3-phase voltage source inverter

Current and voltage waveforms at the output of an inverter are illustrated in Fig. 15. Only the instantaneous values $+V_{DC}$, 0 and $-V_{DC}$ can be applied across the two motor terminals, and these are alternately switched by the GTOs and diodes.
The sinusoidal waveform of the motor average voltage (its fundamental value V_1), is simulated by modulating the voltage pulse width across a half period of motor frequency, as clearly shown. Thus, the mean value of each individual pulse is equal to the instantaneous value of the simulated motor waveform. This technique is called PWM (**P**ulse **W**idth **M**odulation). The higher the switching frequency, the better the sine wave simulation, and the smoother the motor will operate (reduced torque pulsations, less noise, increased motor lifetime and higher efficiency).

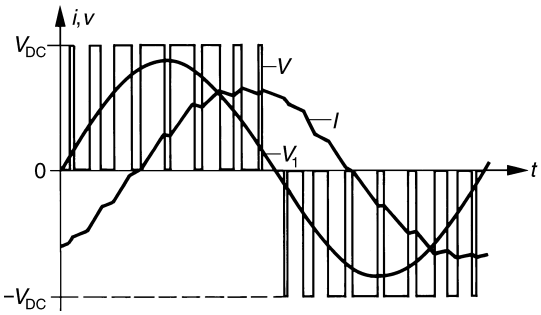


Fig. 15

Load Current I, Load Voltage V and its fundamental Component V1 at the Output of Inverter, Fig.14.

5.7 Protective Circuits

With conventionally controlled GTOs (“soft” turn-on and turn-off), supplementary di/dt and dv/dt limitation networks must be incorporated.
Fig. 16 illustrates typical di/dt and dv/dt snubbers for a DC chopper.

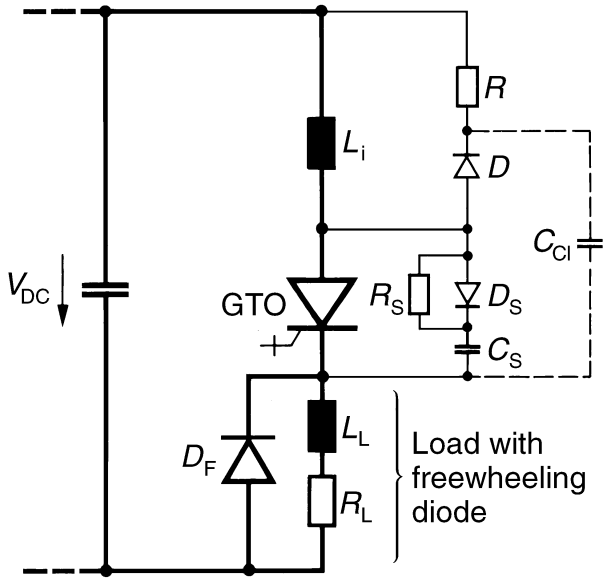


Fig. 16

GTO Protection Circuits:
- Turn-on protection (L_i, R, D)
- Turn-off protection (D_s, C_s, R_s, C_{cl})

5.7.1 Turn-On Protection

Inductance L_i, in series with the GTO, limits di/dt to approx. V_{DC} / L_i
In so doing, it traps energy $E = ½ \bullet L_i \bullet I^2$ which, at turn-off, will cause an overvoltage:

$$\Delta V = \sqrt{L_i / C_s}\ .$$

If this is unacceptable, the over-voltage ΔV can be clamped with an RD circuit as shown in Fig. 16.
R_S limits the discharge current from the dv/dt limiting capacitor C_S at turn-on, thus preventing the formation of hot-spots and eventual device damage. C_S must be discharged within the minimum turn-on time $t_{on\ (min)}$, determined by the application. A rule of thumb is: $R_S \bullet C_S \leq t_{on\ (min)}/5$.

5.7.2 Turn- Off Protection

The turn-off process is illustrated in Fig. 17. GTO anode current falls typically at a rate of several thousand amps per microsecond and, since the inductive load current remains constant, this current commutates with the same high di/dt into the snubber circuit. For the snubber circuit to effectively play its role of limiting the rate of voltage rise, it must be *of very low impedance*. In the forward direction, the snubber resistor R_s is short-circuited by the diode D_s so that, in principal, only the capacitor C_s is present across the GTO, establishing the dv/dt at approximately I_{tgq}/C_s. Due to wiring inductance, however, as well as *forward recovery voltage* of diode D_s (see Section 3), a fast rising voltage spike V_{dsp} is initially generated (see Fig. 17).

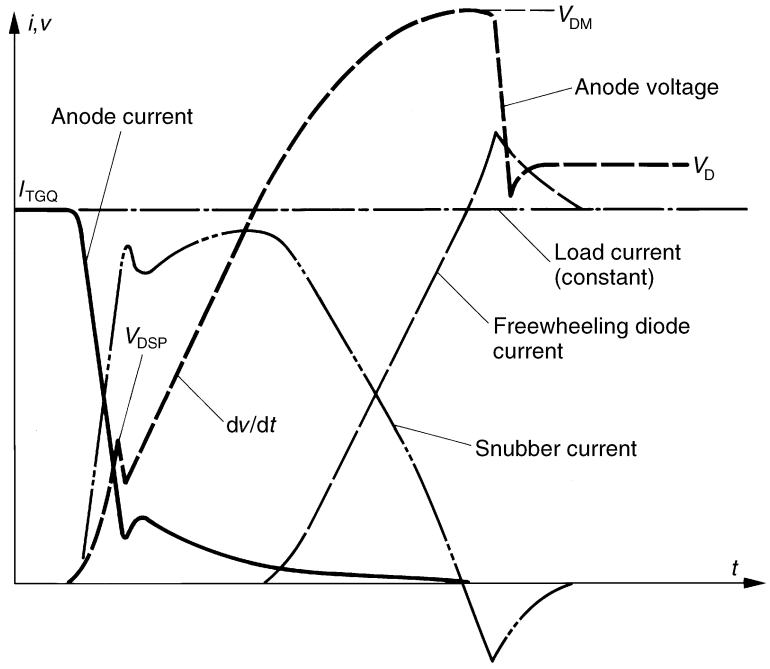


Fig. 17 Current and Voltage Waveforms at GTO Turn-off in the circuit of Fig. 16

Stray inductance should be less than 300 nH, and a careful design will typically yield values below 150 nH. As an example, at 3 kA/µs, a typical 4.5 kV snubber diode will produce a forward recovery voltage spike of about 400 V, and a 150 nH snubber inductance one of 450 V, resulting in a V_{dsp} of 850 V superimposed on the I_{tgq}/C_s ramp. As can be seen from Fig.17, this spike occurs at an instant when there is still considerable current, hence charge carriers in the anode, which modulate the space charge. An excessive value of V_{dsp} coupled with a filamentating cathode current, may cause "dynamic avalanche" and lead to device destruction. In some cases it may be desirable to further limit V_d with an additional clamping capacitor C_{cl}, (see Fig. 16). This capacitor is connected in parallel with the GTO via a diode (i.e. the L_i snubber diode D). For $V_d > V_{dc}$, C_{cl} is initially in parallel with C_s and can discharge through R to V_{dc}. Thus, some of the capacitive energy is dissipated in R while a part is restored to the DC link capacitor.
The above described snubber circuit is designated “RCD”. It suffers from the disadvantage of relatively large power losses at high frequencies, according to the equation: $P_v = ½ \cdot f \cdot C_s \cdot V^2$. More popular approaches are the McMurray, and Undeland/Marquardt circuits [6].

5.8 Series and Parallel Connection

The simplest approach to series or parallel connections, in reality, is the interconnection of complete converters (Fig. 18a). This is, however, the least economical. Fig. 18 shows the principals involved and these are elaborated below.

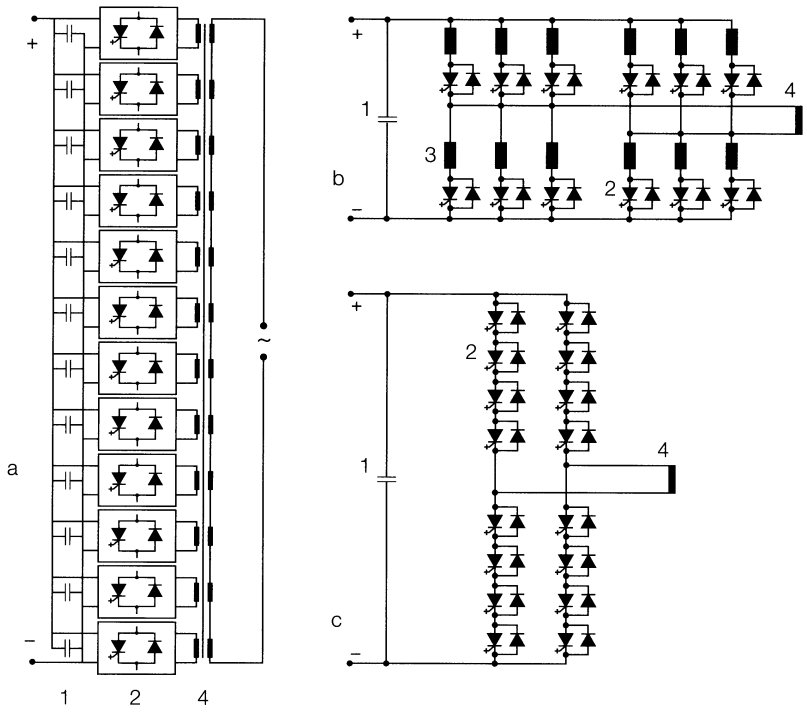


Fig. 18 a) Interconnection of converters; b) Parallel connection of device
c) Series connection of devices
1) DC-link capacitors; 2) GTOs; 3) Sharing Impedance; 4) Load

5.8.1 Series Connection

Traditionally, the series connection of GTOs has been difficult to accomplish, due to the long storage times of conventional GTOs -- in the order of 25 µs. Assuming a parametric dispersion of, say, ±10%, this would still allow a spread of 5 µs between the fastest and the slowest device to turn off. If conventional 3 kA/4.5 kV GTOs were to be series connected using 6 µF snubbers, the resulting out-of-balance voltage would be:

$$\Delta V = 1/C_s * I_{TGQ} * \Delta t_s$$

where: C_s is the snubber capacitance (= 6 µF)
I_{TGQ} is the turn-off current (=3000 A)
Δt_s is the spread in storage time (= 5 µs)

In this case, ΔV_s = 2500 V, which is more than half the rated voltage of the chosen devices: a very uneconomical approach. Fig 20 illustrates poor voltage sharing in a series stack of 3 GTOs.
An alternative method of addressing series operation is adaptive gate control, where the turn-off timing is individually and automatically adjusted for each individual device, so that the resultant re-applied voltage is the same for each device in the series stack. This technology works well but is complex and costly.
The preferred solution is to specify use of GCTs [5]. The hard-drive commutation mode shrinks device storage times to about 1 µs, such that a ±10% spread results in a Δts of only 200 ns yielding a ΔV of only 100 V in the above example.

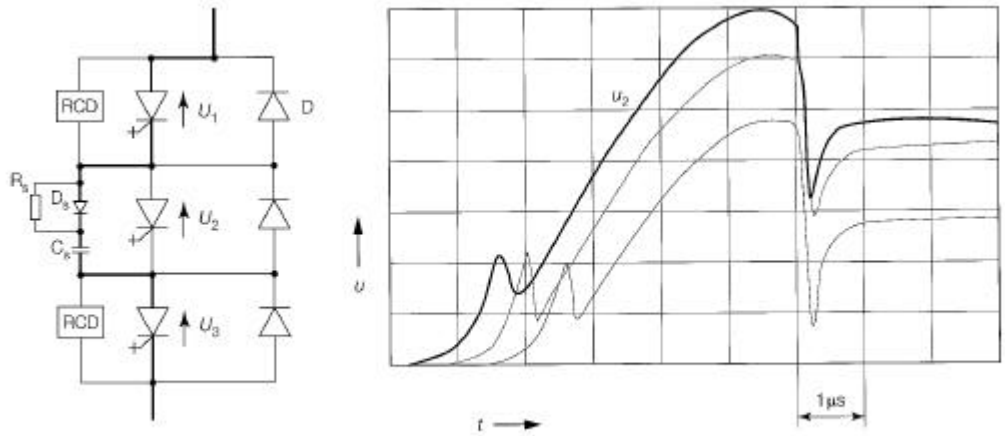


Fig. 19 Turn-off of 3 Series Connected GTOs without Hard-Drive or Adaptive Gate Control

Turn-on presents similar, but less acute difficulties, since the sum of gate delay and rise times ($t_d + t_r$) is only about one third of the storage time, and the same snubber is active during turn-on as for turn-off. Increasing gate drive at turn-on reduces both t_d and t_r so, once again, use of a GCT instead of a GTO, greatly facilitates turn-on voltage sharing by supplying I_{GM} values of several hundred amps from a low voltage source. At these values of I_{GM}, ($t_d + t_r$) is no more than a few hundred nanoseconds, such that a ±10% parametric dispersion is unimportant.

5.8.2 Parallel Connection

Because today's GTOs can switch currents of 4 to 6 kAs, it is rarely necessary to envisage paralleling these devices. However, certain applications, such as static circuit breakers, do exist where parallel operation may be needed.
Little work has been published on the direct paralleling of GTOs at the time of writing*, so only general observations can be made here*. The parallel operation of bipolar semiconductors is generally feasible, albeit problematic, but comparisons with other semiconductor types may suggest possible approaches:

Bipolar transistors have traditionally been parallel operated, but they differ greatly from thyristors, in that their turn-on differences are due to gain dispersion, which become insignificant at low values of forced gain. Thyristors are usually turned on in a regenerative switch mode, in which the *current dependent* gains of *two* constituent transistors determine turn-on rates. (Additionally, most thyristors have amplifying gates. If the "pilot" thyristor has insufficient anode voltage during its delay time - as may happen in an unstable parallel combination - it may never trigger at all.) Since dynamic turn-on sharing is better with non-amplifying rather than amplifying gate thyristors, and that, further, transistors are simpler still, it may be concluded **empirically** that IGCTs, hard-driven in the transistor mode, are *potentially* suitable for parallel connection.

The conduction phase also poses sharing problems. At low current levels, on-state voltages decrease with increasing temperature leading to unstable current sharing. There exists a certain level of current at which there is no temperature dependence. This is known as the *cross-over point* above which the on-state voltage temperature-coefficient is positive (see the on-state characteristics in the data sheets). A low cross-over point increases the range of currents over which *stable* (though not perfect) current sharing may be expected. Over this range, on-state voltage selections will allow predictable current sharing.

The most critical phase of parallel operation is, once more, *turn-off*.
Again, it must be stressed at this point, that *insufficient data for parallel operation exists,* but it seems reasonable to assume that minimising turn-off delays, and hence their dispersion, will minimise the amount of current re-distribution which will occur between devices at turn-off.

A small amount of inductance in series with the individual anodes will also force sharing during this phase, but will also increase turn-off losses. Such an increase in losses, in any event, is not likely to pose problems in low frequency or “single shot” (circuit breaker) applications. Where discrete inductances are used, they will also have a finite resistance, which will further enhance sharing during static conduction (Fig. 18b).

5.9 Product Types

The present range of ABB Semiconductors’ devices is described in Section 1, along with a description of the part numbering system. Basically, the range of products consists of:

- Conventional Asymmetric GTOs (2.5 to 4.5 kV)
- Buffer Layer GTOs (4.5 kV)
- Transparent Emitter GTOs (4.5 to 6 kV)
- Reverse Conducting GTOs (4.5 kV)
- Gate-Commutated Thyristors GCTs (4.5 kV)
- Snubber Diodes (2.5 to 6 kV)
- Free-Wheel Diodes (2.5 to 6 kV)

For detailed descriptions of the above products, see Sections 1 and 2.
Future products will include reverse conducting GCTs, reverse blocking GTOs up to 6 kV, and free-wheel diodes for snubberless operation.

Each of the above device types has its preferred area of application, which can briefly be summarised as:

- Conventional Asymmetric GTOs for present 2.5 kV and 4.5 kV applications, require standard snubbers (500 V/μs)
- TGTOs: 4.5 kV for very low loss applications, standard snubbers (500 V/μs); 6 kV for all applications
- Fine Pattern Buffer-Layer GTOs: low-loss, reduced snubbers for new 4.5 kV applications (1000 V/μs)
- Reverse Conducting GTOs: for compact designs (1000 V/μs)
- GCTs for series or snubberless operation (3000 V/μs)

5.10 Outlook

The performance of GTO based devices continues to improve dramatically. The reverse conducting GCT, with transparent emitter technology, allows:

- high currents (I_{TGQ}, I_{rms}, $\hat{I}_{pulse}$)
- high voltages (static and dynamic)
- fast switching (t_d, t_r, t_s, t_q, $t_{on\text{-}min}$, $t_{off\text{-}min}$, dv/dt)
- low losses (V_T, E_{on}, E_{off})
- high frequency for applications > 2000 V
- high reliability (FITs, thermal cycling, stability, low parts count)
- compact and economical snubberless constructions
- simple series connections for emerging very high power applications.

Developments in companion fast recovery diodes, for free-wheel and neutral-point clamping, will match the progress being made in active switches, to allow snubberless operation at high values of di/dt.
New applications are now emerging in areas such as Power Transmission and Distribution, Marine Drives, and Medium Voltage Industrial Drives where gate turn-off semiconductors could not previously be envisioned for reasons of cost, reliability or efficiency.

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