SECTION 3

DATA SHEET USER'S GUIDE

BY ANTON SCHWEIZER

DATA SHEET

USER'S GUIDE

3.1 GTOs Introduction

This section is a detailed guide to proper understanding of a GTO data sheet. Parameters and ratings will be defined, and illustrated by figures where appropriate. The same sequence will be followed as on the data sheets. For purposes of explanation, data associated with a GTO type 5SGA 30J4502 have been used. In that other devices have similar data sheets, this guide is applicable to all conventional GTOs, and to a great extent also, to hard-driven GCTs (gate commutated thyristors). A 5SGY 35L4502 is used as the model in this latter case, and the specifics associated with it will be covered at the end of the section.

All references to figures refer to the *figures in this section*, unless otherwise noted. In cases where figures have been reproduced from the 5SGA 30J4502 data sheet, this has been noted.

Guide to the 5SGA 30J4502 data sheet

General note: Unless explicitly mentioned in the conditions, all data given in the data sheets applies over the entire operating temperature range of -40 °C to 125 °C.

Key Parameters

V_{DRM}	=	4500	V
I_{TGQM}	=	3000	A
I_{TSM}	=	24	kA
V_{TO}	=	2.20	V
r_T	=	0.60	mΩ
$V_{DC\text{-}link}$	=	2800	V

Gate turn-off Thyristor

5SGA 30J4502

Doc. No. 5SYA 1202-02 Oct.96

These *key parameters* roughly identify the GTO without reference to operating conditions. All data presented here also appears in the appropriate section of the data sheet, together with relevant conditions. For example, I_{TSM} = *24 kA* can also be found in the on-state section, and it can be seen that this value applies at t_p = 10 ms and T_j = 125 °C, with zero reapplied voltage.

Features

- **Patented free-floating silicon technology**
- **Low on-state and switching losses**
- **Annular gate electrode**
- **Industry standard housing**
- **Cosmic radiation withstand rating**

The *features* highlight salient technology of the device. Detailed information about GTO design and technology is given in Section 2, "Product Design". The following is a brief synopsis of some features that are common to most GTOs:-

- *Patented free-floating silicon technology*

Free-floating silicon technology refers to a silicon wafer that is not alloyed to adjacent molybdenum discs, inside the press-pack housing. Thus, electrical and thermal contacts are made by external mounting force only. The advantage of this technology to the user, is that cost effective and modern wafer manufacturing processes can be adopted, which favour optimum trade-offs between static and dynamic parameters. Also, process variations and associated parameter shifts are reduced, compared to alloyed wafers.
ABB was among the first semiconductor companies to use free floating technology for the manufacture of high power GTOs, and this advanced technology has since become a world standard. Even more than conventional thyristors, GTOs have a fine structured anode design, which would not be manufacturable using alloy technology. See also Section 2, "Product Design".

- *Low on-state and switching losses*

Thanks to free-floating technology, it is possible to reduce device thickness for a given blocking voltage, thereby reducing on-state voltage and/or turn-off energy. Further improvements have recently been achieved on some devices, by introducing an n-doped buffer layer on the anode side, in order to have a trapezoidal rather than a triangular field distribution, to complement the so-called transparent emitter anode design.

- *Annular gate electrode*

While small GTOs, with a turn-off current up to about 1500 A, can be turned off with a central gate contact, high power GTOs need an annular gate electrode. This is to channel the necessary high gate current at turn-off, to the innermost and outermost cathode segment rings. This ensures that all segments are able to switch homogeneously at the same time, and prevents damage to wafer metallization near the gate electrode, due to excessive current densities.

- *Industry standard housing*

GTOs, like all high power semiconductors, are often exposed to dirty and aggressive environments, which would deteriorate long-term blocking behaviour and other important device characteristics, if the silicon wafer were not protected by a hermetically sealed ceramic housing. Before sealing, the housing is filled with nitrogen, which inhibits oxidation of the metal parts inside. Nitrogen guarantees excellent blocking stability over several decades of expected device lifetime.
Depending on the device type, two different sealing techniques are used: cold-welding and plasma-welding. Additional information on the housing is given later in this section.

- *Cosmic radiation withstand rating*

As explained in Section 2, in the early 1990`s it was found that cosmic particles can lead to random destruction of power semiconductors exposed to high blocking voltages for long periods. Interestingly, the failure rate is independent of junction temperature.
Although this phenomenon exists for all power semiconductors, it was not a problem in the past. Traditionally, diodes and thyristors were exposed to AC voltages, with an average voltage stress far below their peak voltage capability. In modern DC-link converters, however, GTOs may be exposed to a high DC voltage of up to 2/3 of V_{DRM}. This can make cosmic radiation a major cause of random failure, unless the design-rules for its avoidance are not followed by the device development engineer. It is important to note that cosmic susceptibility is not limited to GTOs, but applies to all semiconductors exposed to high DC voltages, namely freewheeling diodes and crowbar phase control thyristors.

Blocking

V_{DRM}	Repetitive peak off-state voltage	4500 V	$V_{GR} \geq 2V$
V_{RRM}	Repetitive peak reverse voltage	17 V	
I_{DRM}	Repetitive peak off-state current	≤ 60 mA	$V_D = V_{DRM}$ $V_{GR} \geq 2V$
I_{RRM}	Repetitive peak reverse current	≤ 20 mA	$V_R = V_{RRM}$ $R_{GK} = \infty$
$V_{DC\text{-}link}$	Permanent DC voltage for 100 FIT failure rate	2800 V	Ambient cosmic radiation at sea level, open air

- V_{DRM}

V_{DRM} is the *maximum repetitive voltage* in the *forward direction*. The GTO is able to block this voltage at line frequency, 50 or 60 Hz, assuming a sinusoidal voltage form. V_{DRM} is a maximum rating; when exceeded, leakage current and power loss may increase rapidly, and lead to thermal runaway and subsequent blocking degradation.
Although V_{DRM} specifies the GTO`s quasi-static blocking capability, it is also the maximum dynamic voltage, V_{DM}, that all GTOs from ABB Semiconductors can withstand following turn-off, i.e. $V_{DRM} = V_{DM}$, as indicated in the conditions for the I_{TGQ} definition (see later in this section).
It is important to note that the GTO can only block rated voltage if the gate is reverse biased (e.g. $V_{GR} \geq 2$ V), or at least connected to the cathode through a low value resistor, R_{GC}. More information on this

subject is given later in this section, when Fig. 5 of the 5SGA 30J4502 is explained.

- V_{RRM}

V_{RRM} is the maximum repetitive voltage in the reverse direction. For all asymmetric GTOs, this value is in the range of 17 V, since it is determined by the reverse blocking capability of the gate-to-cathode junction (V_{GRM}).
Unlike V_{DRM}, V_{RRM} may be exceeded for a short time without destroying the GTO, since reverse current flows across the whole thyristor area. This so-called *reverse avalanche capability* is explained in detail later in this section.

- I_{DRM}, I_{RRM}

I_{DRM} and I_{RRM} specify maximum leakage current, when V_{DRM} and V_{RRM} are applied, respectively. They are measured at $T_{j\,max}$, with sinusoidal voltage pulses (t_p = 10 ms) under the specified gate conditions.

- $V_{DC\text{-}link}$

$V_{DC\text{-}link}$ is the maximum continuous DC voltage for a specified failure rate (100 FIT for example), due to cosmic radiation. Exceeding this voltage does not *immediately* lead to device failure, but the probability of a cosmic radiation failure increases progressively with the applied DC voltage. Upon request, ABB Semiconductors is able to calculate the cosmic radiation failure rate for all GTOs and diodes, at any DC voltage, according to a model that has been developed from extensive experimental investigations.

Mechanical data

F_m	Mounting force	min	36 kN
		max	44 kN
a	Acceleration: Device unclamped Device clamped		 50 m/s² 200 m/s²
m	Weight		1.3 kg
D_s	Surface creepage distance		33 mm
D_a	Air strike distance		15 mm

- F_m

F_m is the mounting force necessary to establish a good electrical and thermal contact. It is very important that F_m stay within the specified limits, even under worst case extremes of operating temperature. Thermal expansion, and tolerances of stack parts, have to be considered in the design of the clamping system. Too low a mounting force results in increased thermal resistance and, particularly at high currents, in damage to dry interfaces within the housing, that may provoke degradation. Also, there is a risk that not all individual cathode segments are well contacted, leading to an increase in V_T, and *drastic* reduction of I_{TSM} and I_{TGQM}.

Exceeding F_m leads to increased mechanical stress on the silicon wafer, particularly where thermal cycling is severe. This reduces life-expectancy of the device, and can lead to premature wear-out of the cathode segment metallization, with subsequent gate-to-cathode short circuits.
Besides a correct mounting force, it is also vital that the pressure be distributed homogeneously over the contact area. If not, the copper pole pieces of the housing may be deformed plastically. This, in turn, may lead to local mechanical stresses on the silicon wafer, with subsequent degradation of device performance.
A guide to the correct mounting of a press-pack semiconductor is included in the definition of R_{thCH} later in this section (see Fig. 5).
Note: If no external force is applied across a press-pack semiconductor, the silicon wafer will probably not contact the pole pieces at all. For even the most basic device verifications (blocking or gating checks by service personnel), a minimum clamping force of about 1 kN is required to establish contact for *low*-current measurements.
All the "mechanical" rules associated with thyristors apply to GTOs as well, but it must be emphasized that the GTO, due to its cathode segmentation, is even more sensitive to incorrect mounting. This is underscored by the field failures revealed in failure analyses at ABB Semiconductors.

- *a*

Maximum permissible acceleration in any direction, when the device is clamped with the nominal mounting force.

- *m*

m is the weight (strictly speaking, mass) of the complete device, gate lead included.

- D_s

The surface creepage distance, defined as the *shortest path along the ceramic surface* between the anode flange and the gate contact (see Fig. 1 a).

- D_a

The air strike distance, defined as the *shortest direct path* between the anode side and the gate contact, as illustrated in Fig. 1 b.

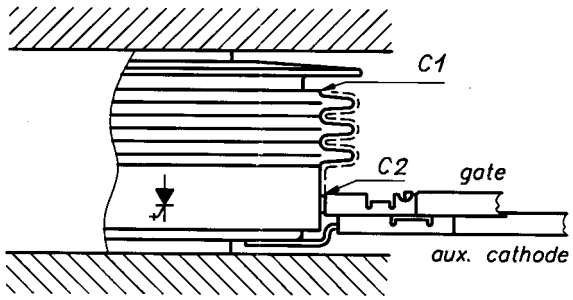

Fig. 1a
Definition of surface creepage distance (D_s): Shortest way fromC1 to C2 *along the ceramic surface.*

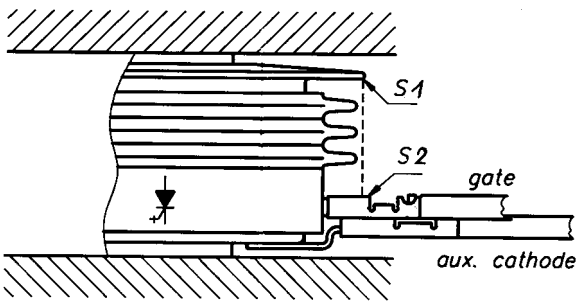

Fig. 1b
Definition of air strike distance (D_a): Shortest *air distance* between S1 and S2.

- *Housing*

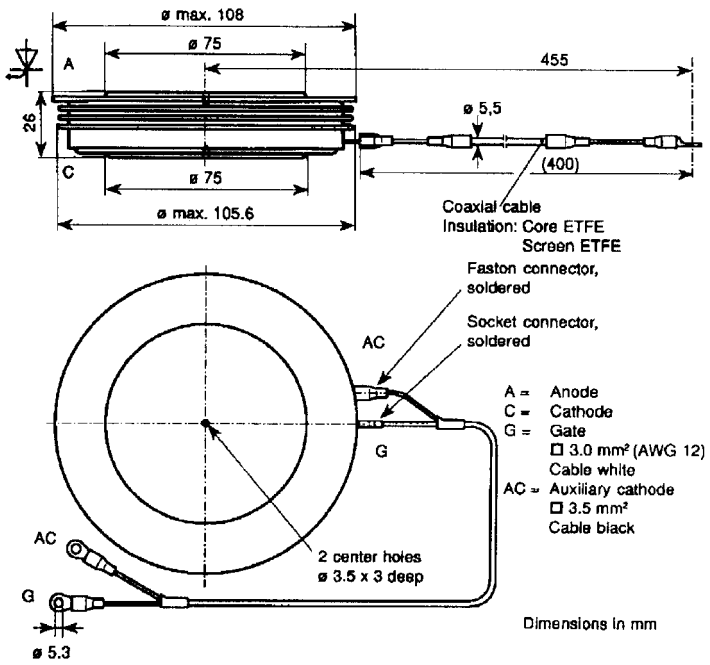

Fig. 2 Outline drawing of the press-pack housing for the 5SGA 30J4502. All dimensions are nominal values in millimetres unless stated otherwise.

The major difference between a GTO housing and a conventional thyristor housing, is in the gate contact and gate lead. Both are much more robust in the GTO, since RMS and peak gate currents may be 2-3 orders of magnitude higher than for a thyristor.
For most applications, the standard coaxial gate lead, as specified in the corresponding outline drawing, is suitable. If for any reason a special gate lead, coaxial or any other type, should be required, ABB Semiconductors is able to customize it according to the customer`s specification.

As is well known, gate lead inductance is a very important parameter, since it largely determines the slope of the negative gate current at turn-off, diGQ/dt. Total gate lead inductance is the sum of the coax cable inductance and the inductance of the loops at both ends. The first is a fixed value, while the latter, which may be half the total value!, depends on the area within the loops. It is therefore vital to minimize the loop area at both ends, when GTOs are being mounted in a converter.

On-state

I_{TAVM}	Max. average on-state current	930 A	Half sine wave, T_c = 85 °C		
I_{TRMS}	Max. RMS on-state current	1460 A			
I_{TSM}	Max. peak non-repetitive surge current	24 kA	t_p =	10 ms	T_j = 125°C
		40 kA	t_p =	1 ms	After surge: $V_D = V_R$ = 0V
I^2t	Limiting load integral	$2.88 \cdot 10^6$ A²s	t_p =	10 ms	
		$0.80 \cdot 10^6$ A²s	t_p =	1 ms	
V_T	On-state voltage	4.00 V	I_T =	3000 A	T_j = 125°C
V_{TO}	Threshold voltage	2.20 V	I_T = 300 - 4000 A		
r_T	Slope resistance	0.60 mΩ			
I_H	Holding current	50 A	T_j = 25°C		

- I_{TAVM}, I_{TRMS}

Max. average and root-mean-square (RMS) on-state currents, respectively.
These values are established with given boundary conditions. The case temperature is fixed at a certain value, say 85 °C, when I_{TAVM} and I_{TRMS} become the average and RMS values of the half-sinusoidal on-state current, that heats up the junction to its maximum temperature of 125 °C.
These figures give an order of magnitude to current handling capability. They are mainly used to compare different products for on-state performance. If such comparisons are made, care must be taken, since the assumed case temperature may differ from product to product, and between suppliers, which substantially influences the current ratings.
The user can easily calculate I_{TAVM} and I_{TRMS}, under varying conditions, from the following equations:

$$I_{TAVM} = 2\frac{\sqrt{V_{T0}{}^2 + r_T \cdot \pi^2 \cdot P_{AVM}} - V_{T0}}{r_T \cdot \pi^2}$$ with:

$$P_{AVM} = \frac{T_{j\max} - T_C}{R_{thJC}}$$

$$I_{TRMS} = I_{TAVM}\frac{\pi}{2}$$

Note:
The definitions for I_{TAVM} and I_{TRMS} originate from classic phase control thyristor practice, which mainly applies to mains frequency applications at 50 and 60 Hz. Since in most GTO applications, the current waveforms are far removed from a sinusoidal shape, and the switching losses are a considerable part of total power losses, I_{TAVM} and I_{TRMS} have no real practical meaning. However, they may be useful for comparison with other products, as mentioned above.

- *I_{TSM}*

Max. non-repetitive surge current for t_p = 10 ms (corresponding to 50 Hz), and t_p = 1 ms. This is the max. allowed peak value of a half-sinusoidal surge current, applied at an instant when the GTO is operating at its maximum junction temperature. Although, in practice, the case temperature prior to a surge is always below 125 °C, both the junction and housing are heated to 125 °C when the surge current is established. This worst-case test condition provides additional margin for the real stress in an application.
During a surge, the junction heats up to a temperature well above its rated maximum value. Therefore, the thyristor is no longer able to block rated voltage, so the I_{TSM} values are valid only for $V_D = V_R \approx 0$ V after the surge.
Though a single surge does not cause any irreversible damage to the silicon wafer, it should not occur too frequently.

- *I^2t*

Limiting surge current load integral. I^2t in fact is an abbreviation and stands for $\int I_T^2\, dt$. This value is derived from the I_{TSM} value discussed above, according to the following expression:

$$I^2t = \int_0^{t_p} {I_T}^2(t)\, dt = \frac{{I_{TSM}}^2 \cdot t_p}{2}$$

The I^2t of a semiconductor fuse must be lower than the maximum I^2t of the GTO to be protected. The reservations applicable for I_{TSM} apply similarly to I^2t.

- *V_T*

V_T is the maximum on-state voltage, at a given on-state current I_T, and at maximum junction temperature. For most GTOs, this is the reference point for V_T-classification, and as such, is measured 100 % during out-going inspection.
V_T is influenced, within limits, by the electron irradiation dose that determines minority carrier lifetime. A low V_T automatically implies a higher Eoff, and vice versa. If a lower V_T than standard is required, the customer can ask for an *adapted standard product* with an optimized V_T.

- V_{T0}, r_T

In many cases it is convenient, and sufficiently accurate, to approximate the on-state characteristic (max. values) by a straight line, characterized by V_{T0} and r_T:

$$V_T(I_T) = V_{T0} + I_T \cdot r_T$$

The current range over which this expression yields acceptable accuracy is indicated by the conditions, that is 300 - 4000 A for the 5SGA 30J4502.
When average and RMS values of on-state current, I_{TAV} and I_{TRMS}, are known, then the on-state power loss, $P_{on\text{-}state}$, is readily calculated using V_{T0} and r_T:

$$P_{on-state} = V_{T0} \cdot I_{TAV} + r_T \cdot I^2_{TRMS}$$

- I_H

I_H is the holding current, defined according to Fig. 3:

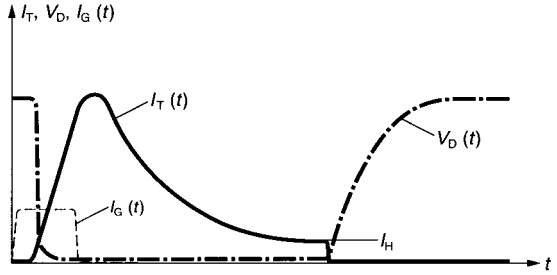

Fig. 3a

Definition of holding current, I_H.
After suppression of gate current, the GTO remains conductive until the anode current falls below I_H.

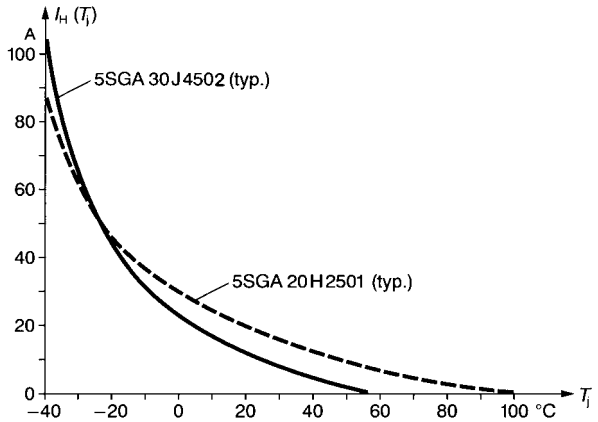

Fig. 3b

Temperature dependence of I_H for two different types of GTO (typical values).

When the GTO is latched in the on-state, gate current is no longer needed to maintain regenerative conduction, providing the anode current exceeds the holding current. If I_T falls below I_H, the GTO reverts to its blocking state, as illustrated in Fig. 3a.
Fig. 3b shows typical values of holding current for two GTO types, between -40 ºC and 100 ºC. In that the temperature dependence of I_H is greatly affected by technology and manufacturing process variations, I_H scatter is considerably higher than for most other parameters. It is evident that I_H increases at low temperatures, in a similar manner to the gate trigger current, I_{GT}.

Since the I_H of a GTO is much higher than that of a thyristor (GTO: 1 - 30 A , thyristor: 0.1 - 1 A typ. at 25 °C), anode current variations can generate serious problems, because the GTO might “un-latch” at an inappropriate moment. These problems can be avoided by feeding a continuous so-called *backporch current* into the gate during the on-state period. This DC gate current should be about 20 % higher than gate trigger current, I_{GT}, at the lowest expected junction temperature, this being worst case.

Gate

V_{GT}	Gate trigger voltage	1.0 V	V_D = 24 V T_j = 25°C
I_{GT}	Gate trigger current	3.0 A	R_A = 0.1 Ω
V_{GRM}	Repetitive peak reverse voltage	17 V	
I_{GRM}	Repetitive peak reverse current	20 mA	$V_{GR} = V_{GRM}$

- *V_{GT}, I_{GT}*

I_{GT} is the gate trigger current, and V_{GT} the instantaneous gate-cathode voltage, when I_{GT} is flowing into the gate. I_{GT} is strongly temperature dependent, as portrayed in Fig. 8 on the 5SGA 30J4502 data sheet.
I_{GT} merely specifies the minimum backporch current necessary to turn on the GTO at low di/dt, and then maintain it in conduction independent of I_T, as described above. When a high power GTO must be switched on with a high anode di/dt (10 A/µs to several 100 A/µs), the supplied gate current should be at least 30 A, with a di_G/dt of 20 A/µs. See the "Turn-on switching" section below.

- *V_{GRM}*

V_{GRM} is the max. repetitive reverse gate voltage. Exceeding V_{GRM} drives the gate-to-cathode pn^+-junction into avalanche breakdown. This is far less dangerous than avalanching the main (anode-to-cathode) junction, as the gate junction is relatively avalanche-proof. V_{GRM} increases by about 0.1 % per °C with rising junction temperature.

- *I_{GRM}*

Repetitive peak reverse gate current (leakage current) at V_{GRM} and $T_{j(max)}$. Because the blocking characteristics of the individual cathode segments have been dramatically improved over the years, typical I_{GR}-values are in the mA, or even µA, range nowadays.

Turn-on switching

di/dt_{crit}	Max. rate of rise of on-state current	400 A/µs	f = 200Hz	I_T = 3000A
		800 A/µs	f = 1Hz	I_{GM} = 30A di_G/dt = 20 A/µs
t_d	Delay time	3 µs	V_D = 0.5 V_{DRM}	T_j = 125 °C
t_r	Rise time	6 µs	I_T = 3000 A	di/dt = 200 A/µs
t_{on} (min)	Min. on-time	100 µs	I_{GM} = 30 A	di_G/dt = 20 A/µs
E_{on}	Turn-on energy per pulse	3.6 Ws	C_s = 6 µF	R_s = 5 Ω

The definitions of turn-on and turn-off switching parameters, to be elaborated here, are illustrated on the last page of the GTO data

sheets, with typical anode and gate circuit voltage/current waveforms. These waveforms are reproduced in figure 4.

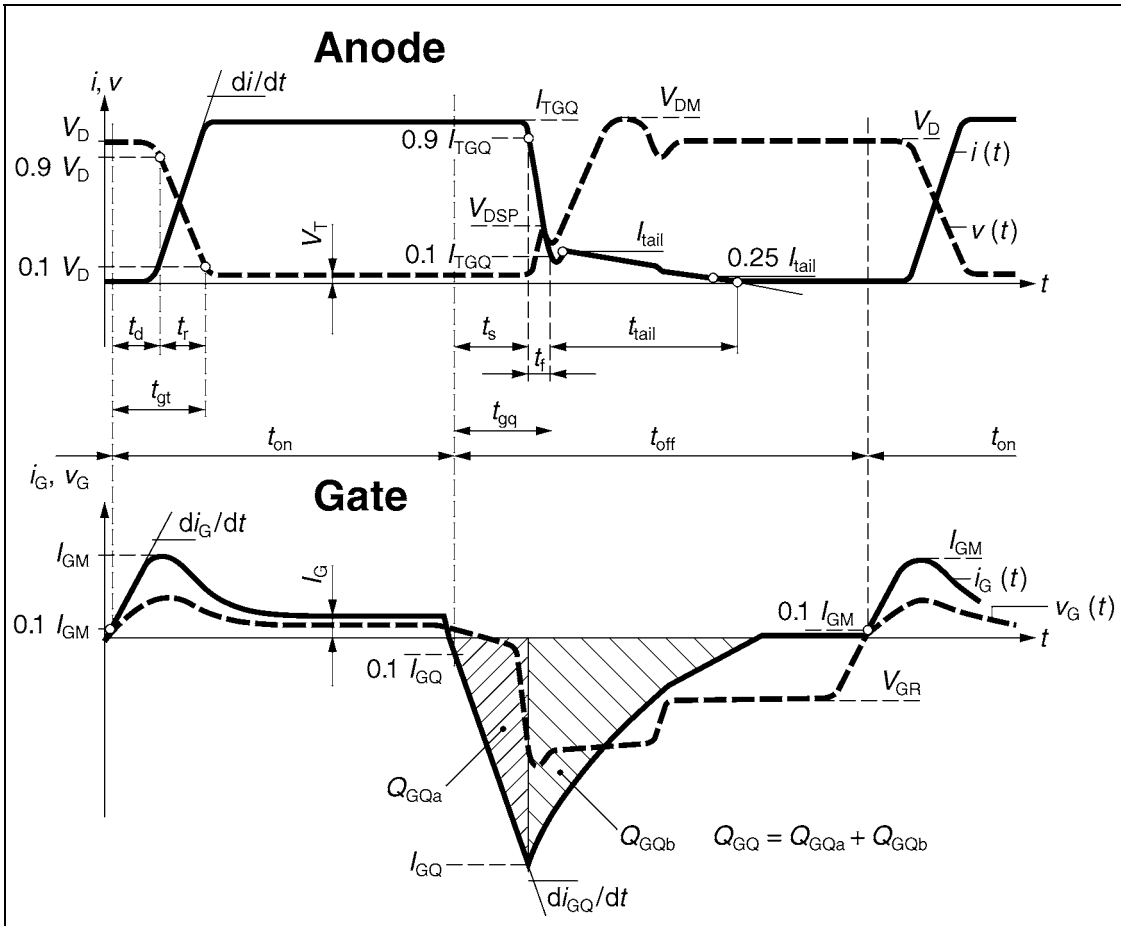

Fig. 4 Typical GTO anode circuit current and voltage waveforms (upper traces), and gate circuit waveforms (lower traces), with corresponding parameter definitions.

- *di/dt_{crit}*

Maximum permissible on-state di/dt at turn-on. One value is given for repetitive operation, f= 200 Hz for example, and one for single pulse operation. The maximum di/dt is very much gate current dependent (rate of rise of gate current di_G/dt, and peak gate current amplitude I_{GM}), as specified in the operating conditions. A substantial gate current ensures that all GTO cathode segments are turned on simultaneously, and within a short time, so that the critical transition from transistor to thyristor operation does not create local hot spots, which could destroy the GTO. The di_G/dt and I_{GM} specified in the operating conditions should therefore be considered as minimum values, and they should be increased whenever a high di/dt is required. Also, Eon is reduced when the gate is driven hard in this way.

- *t_d, t_r*

Turn-on delay time and anode voltage fall time, respectively. These definitions are illustrated in fig. 4. Both t_d and t_r can be influenced in a positive way by the user: a meaty gate current (high di_G/dt and I_{GM}) reduces turn-on switching time. The relationship between t_d, t_r and I_{GM} for the 5SGA 30J4502 is depicted in Fig. 11 on the data sheet, and will be commented on later in this section. A high gate current not only reduces turn-on switching times, but also variations between individual devices. This is especially important when GTOs are to be connected in series, or if low jitter is needed for other reasons (e.g. harmonic distortion).

- *$t_{on(min)}$*

$t_{on(min)}$ is the minimum time that the GTO requires to establish homogeneous anode current conduction. This time is also necessary for the GTO to be able to turn off its rated anode current, under the specified conditions.
Normally, the GTO is connected to a snubber circuit for turn-off protection. During the on-state, the snubber capacitor must be discharged, so it is ready for dv/dt-protection at turn-off. Therefore, another minimum on-time, $t_{on(min)}$*, is required so the snubber may recover. As an example, if an RCD snubber with R_s = 5 Ω and C_s = 6 µF is used, a $t_{on(min)}$* of approximately $4 \cdot R_s \cdot C_s$ = 120 µs would be needed to discharge C_s to 1.8 % of its initial voltage. *In the GTO data sheet, $t_{on(min)}$ only specifies the minimum on-time required by the GTO.* The user must himself calculate $t_{on(min)}$* for the snubber circuit, and take care that the control logic is compatible with both $t_{on(min)}$ (GTO) and $t_{on(min)}$* (snubber).

- *E_{on}*

Turn-on energy per pulse. E_{on} is defined as the time integral of power $P(t) = I_T(t) \cdot V_T(t)$, over a specified integration time (normally 20 µs) :

$$E_{on} = \int_{(20\mu s)} I_T(t) \cdot V_T(t)\, dt$$

Measurement of E_{on} is performed routinely in production, according to the above definition, with a computer controlled, fast sampling high precision oscilloscope.
As mentioned earlier for t_d and t_r, E_{on} can be reduced by driving the gate hard. This is defined for the 5SGA 30J4502 on Fig. 11 in the data sheet.
The turn-on power losses, $P_{turn\text{-}on}$, are calculated as follows :-

$$P_{turn-on} = f \cdot E_{on}$$

where f = switching frequency.

Turn-off switching

I_{TGQM}	Max. controllable turn-off current	3000 A	V_{DM} = V_{DRM} C_s = 6 µF	di_{GQ}/dt = 40 A/µs L_s = 0.3 µH
t_s	Storage time	25 µs	V_D = 0.5 V_{DRM}	V_{DM} = V_{DRM}
t_f	Fall time	3.0 µs	T_j = 125 °C	
t_{off} (min)	Min. off-time	80 µs	I_{TGQ} = I_{TGQM}	di_{GQ}/dt = 40 A/µs
E_{off}	Turn-off energy per pulse	12 Ws	C_s = 6 µF	R_s = 5 Ω
I_{GQM}	Peak turn-off gate current	800 A	L_s = 0.3 µH	

- *I_{TGQM}*

I_{TGQM} is the maximum anode current that can be repetitively turned off by a negative gate current. I_{TGQM} is a function of the snubber capacitor C_s (see Fig. 14 in the 5SGA 30J4502 data sheet), and also dependent on snubber stray inductance L_s, which should be less than 0.3 µH.
C_s limits the dv/dt at turn-off, and low snubber inductance limits the over-voltage spike, V_{DSP}. Both excessive dv/dt and V_{DSP} can lead to dynamic avalanche breakdown, because a relatively high anode current (I_{tail}) is still flowing as voltage rises across the GTO. This current consists of holes, that modulate the space charge region and reduce the dynamic blocking voltage.
di_{GQ}/dt is also an important parameter for I_{TGQM}: high values (≥ 30 A/µs) ensure a low transition time from thyristor to transistor operation (i.e. on-state to off-state), which is very important for a safe, homogeneous turn-off process. There is no upper limit for diGQ/dt. Very high values (several 100 to 1000 A/µs) increase I_{TGQM} considerably; this mode of operation is called "hard drive", and bestows substantial switching improvements in many respects (see description of GCT later in this section).
At ABB Semiconductors, I_{TGQM} is measured routinely three times on every GTO : as a wafer (single pulse), as an encapsulated device in the frequency test (typically 200 Hz), and at final inspection (single pulse). These tests are all effected under limit conditions.

- *t_s*

Storage time is the time between the start of negative gate current and the decrease in anode current, as described in Fig. 4. The following parameters influence t_s: higher values of I_{TGQ} and T_j increase t_s, whereas high di_{GQ}/dt lowers it. See the appropriate figures in the data sheets.
Storage time is one of the most important parameters to be considered in the design of a GTO converter. It plays an important role in the control of GTOs, and can create a number of problems if not properly assessed. Possible issues are shoot through in inverter phase legs (if one GTO does not turn off before the other turns on), and harmonic distortion due to t_s-jitter. Close attention must be given to t_s when GTOs are to be connected in series. Here, variations in ts may lead to unacceptable voltage asymmetries at turn off, with over-voltages appearing on those devices which turn off first. In this case, "hard drive" may be the best solution.

Like V_T and E_{off}, t_s can be influenced to a certain extent, by the dose of electron irradiation. A lower value for t_s means also a lower E_{off}, but a higher V_T, and vice versa. A customized t_s can be specified for an *adapted standard product*.

- t_f

t_f is the fall time of the anode current. It cannot be much influenced, either during manufacturing (e.g. by electron irradiation), or by gate control (e.g. by di_{GQ}/dt). Also, since tf is not strongly dependent on other parameters, dependency curves are not given on the data sheets.

- $t_{off\ (min)}$

Minimum turn-off time, before the GTO may be triggered again by a positive gate current. If the device is re-triggered during this time, there is a certain risk of localized turn-on, and destruction may result. However, if the gate trigger pulse is high enough (e.g. as specified for the turn-on parameters), $t_{off\ (min)}$ may be shorter than specified. Ask ABB Semiconductors` application engineers for assistance, if this parameter is critical in a specific application.

- E_{off}

Turn-off energy per pulse. E_{off} is defined as the time integral of the power $P(t) = I_T(t) \cdot V_D(t)$, over a specified integration time (normally 40 µs):

$$E_{off} = \int_{(40\mu s)} I_T(t) \cdot V_D(t)\, dt$$

E_{off} is measured routinely in production, according to the above definition, with a computer controlled, fast sampling high precision oscilloscope.
The turn-off power losses, $P_{turn\text{-}off}$, are calculated as follows:

$$P_{turn-off} = f \cdot E_{off}$$

with f = switching frequency.

E_{off} can be controlled to a certain extent by electron irradiation, as described earlier in this section for V_T and t_s. If a lower than standard E_{off} is required for a particular application, an *adapted standard product* can be requested.
Gate control at turn-off has only a minor influence on E_{off}, although low di_{GQ}/dt slightly reduces E_{off}. This should not be used as an argument to decrease di_{GQ}/dt, however, as a low di_{GQ}/dt reduces the turn-off safety margin considerably. In contrast, E_{off} is strongly dependent on I_{TGQ}, C_s and T_j, as illustrated in figures 12 to 15 on the 5SGA 30J4502 data sheet.

- I_{GQM}

I_{GQM} is the maximum negative turn-off gate current. It is a very important parameter for gate unit design, since this circuit must be able to deliver the required negative gate current at any time under worst-case conditions (maximum I_{TGQ}, di_{GQ}/dt and T_j). If the gate unit itself limited I_{GQM}, this would considerably increase the storage time t_s, and seriously compromise the turn-off process. This situation must be avoided at all cost.
I_{GQM} is mainly dependent on di_{GQ}/dt, I_{TGQ} and T_j, as illustrated in figures 15 to 17 on the 5SGA 30J4502 data sheet.

Thermal

T_j	Storage and operating junction temperature range	-40.. .. 125°C	
R_{thJC}	Thermal resistance junction to case	22 K/kW	Anode side cooled
		27 K/kW	Cathode side cooled
		12 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	6 K/kW	Single side cooled
		3 K/kW	Double side cooled

- T_j

Storage and operating temperature range. At the lower end, T_j is mainly limited by the difficulty in turning on GTOs at low temperature, i.e. I_{GT}, I_L and I_H increase rapidly as T_j falls below -40 °C. The upper limit, on the other hand, is determined by the blocking capability of the main pn junction. Leakage current rises exponentially with temperature, and thermal instabilities start to manifest above 125 °C. Experiments have shown that $T_{j\ max}$ should not be exceeded, even in the absence of blocking voltage, because wafer edge passivation may suffer from excessive temperature, which may cause increased leakage currents, and subsequent blocking instabilities. This is especially important when endurance or burn-in tests are carried out.

- R_{thJC}

R_{thJC} is the thermal resistance from junction (silicon wafer) to case, that is the surface of the copper pole pieces. Three values are specified on the data sheet: two for single-side cooling (either anode or cathode), and one for double-side cooling. It can be seen that, in most cases, the thermal resistance on the anode side is lower than on the cathode side. This is because, firstly, in cathode side cooling the heat generated inside the silicon wafer must flow through the cathode segments, whose total area is only a fraction of the anode surface, and secondly, the thickness of the anode side copper pole piece is generally less than that of the cathode side, the latter one having to accommodate the bulky gate contact. For this reason, if single-sided cooling is required, we recommend cooling the anode side.
As a free-floating GTO has several dry interfaces inside the ceramic housing, it is self-evident that R_{thJC} is dependent on F_m.

Data sheet figures are therefore based on the nominal mounting force, as specified in the Mechanical Data sub-section. It has already been mentioned that homogeneous mounting pressure is vital for reliable GTO operation; this is particularly important for R_{thJC}.

- *R_{thCH}*

Thermal resistance from case to heat sink (surface of GTO housing to surface of heat sink), is defined with the nominal mounting force F_m applied. Since R_{thCH} is a dry interface between two surfaces, it depends a great deal on the quality of the surfaces, and on homogeneity of the mounting pressure. The specified R_{thCH} is achieved when the heat sink surface is of a similar quality to the GTO surface, that is flatness in the order of 15 µm, roughness in the order of 1 µm, and with the per-unit- area mounting pressure uniform across the surface within ± 15 %. The latter requirement calls for careful design of the clamping system; in particular, it is important that one contact plate is free to pivot, so that it can conform to any non-parallelism of the constituent parts (heat sinks, presspack housings, connection plates, etc.). See fig. 5 for a typical assembly.

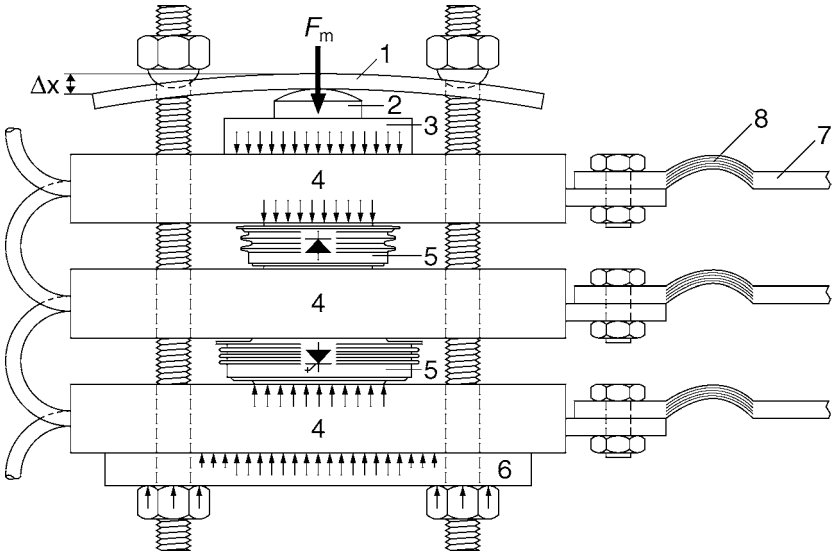

Fig. 5
Example of a stack, illustrating the basic rules for correct clamping of presspack semiconductors:

1. Leaf spring. Spring excursion Δx must be great in comparison with thermal expansion of stack parts in order to keep F_m constant over time and temperature variations.
2. Spherical cup ensures that F_m is transferred symmetrically to the semiconductors and allows the parts within the stack to adapt to inherently present non-parallelisms.
3. Strong steel plate for homogeneous pressure transfer to heat sink (4), symbolised by small arrows.
4. High-quality heat sink: Clean, parallel and flat surfaces, roughness ≈ 1 µm.
5. Presspack semiconductor: Surfaces cleaned and covered with thin film of silicone oil before mounting.
6. Strong yoke ensures homogeneous pressure distribution on heat sink (4), symbolised by small arrows.
7. Bus bars (7) connected to heat sinks (4) by means of flexible connections (8) to avoid that uncontrolled "external" forces disturb the homogeneous pressure distribution within the stack.

Before mounting the stack parts in the clamping system, the various surfaces should be cleaned with alcohol or similar, and it may be advantageous to lubricate them with a *thin* film of silicone oil to improve the thermal contact, and to prevent oxidation if the stack is exposed to an aggressive environment. However, silicone oil or contact grease will never compensate for poor-quality heat sink surfaces!

ABB Semiconductors operates a state-of-the-art failure analysis laboratory for analysing semiconductor defects including field failures. Years of experience show that mechanical issues such as clamping system design or assembly procedure are often the root cause of failure. One method of checking for homogeneous mounting pressure is to clamp a pressure-sensitive paper between the surfaces. The film changes colour and colour density is then a measure of the mounting pressure. This method is cheap, simple and fast and even allows rough scaling of the static pressure distribution.

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^{4} R_i(1-e^{-t/\tau_i})$$

i	1	2	3	4
R_i (K/kW)	5.4	4.5	1.7	0.4
τ_i (s)	1.2	0.17	0.01	0.001

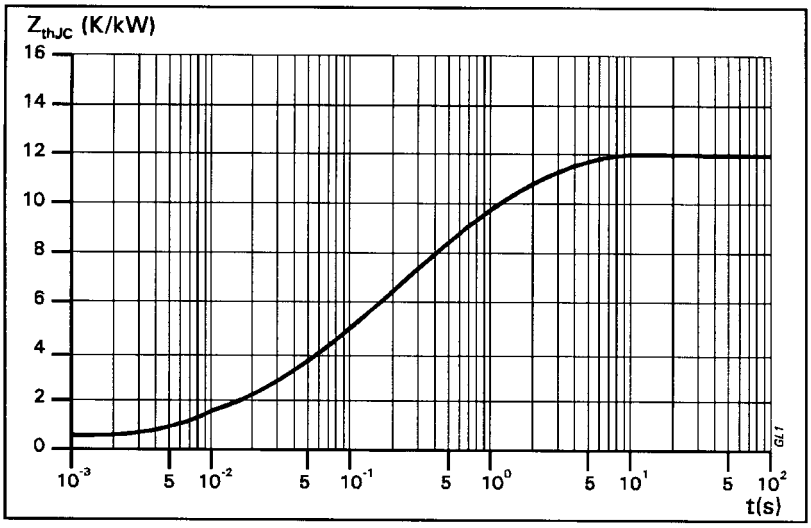

Fig. 6 Transient thermal impedance, junction-to-case. Both the analytical expression and the curve specify Z_{thJC} (t) for double-sided cooling, with the nominal mounting force of Fm = 32 kN applied. This figure corresponds to Fig. 1 of the 5SGA 30J4502 data sheet.

Transient thermal impedance, Z_{thJC} (t), characterizes the rise of junction temperature versus time, when constant power is dissipated in the junction. It is defined as the temperature difference, junction-to-case, divided by the power:

$$Z_{th\,JC}(t) = \frac{\Delta T_{JC}(t)}{P}$$

This function can be specified as a curve (see below), or by an analytical approximation with the superposition of four exponential terms, as listed above. The analytical expression is useful for computer calculations.

On-state characteristics

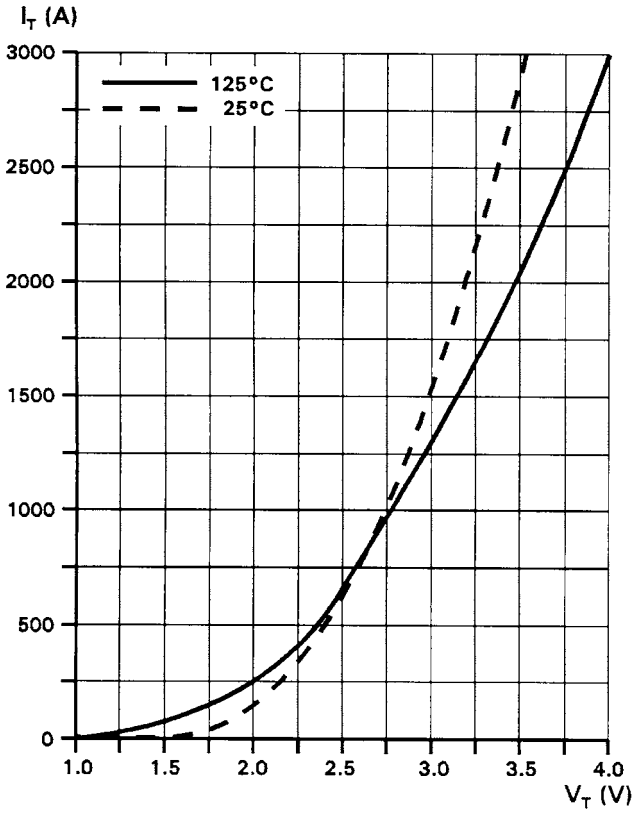

Fig. 7 On-state characteristics (maximum values). This figure corresponds to Fig. 2 of the 5SGA 30J4502 data sheet.

Fig. 7 shows maximum on-state voltage vs. on-state current, for T_j = 25 °C and 125 °C. These curves are used to calculate on-state losses; the 125 °C curve can also be approximated by a straight line, characterized by V_{T0} and r_T, as discussed in the on-state parameters.

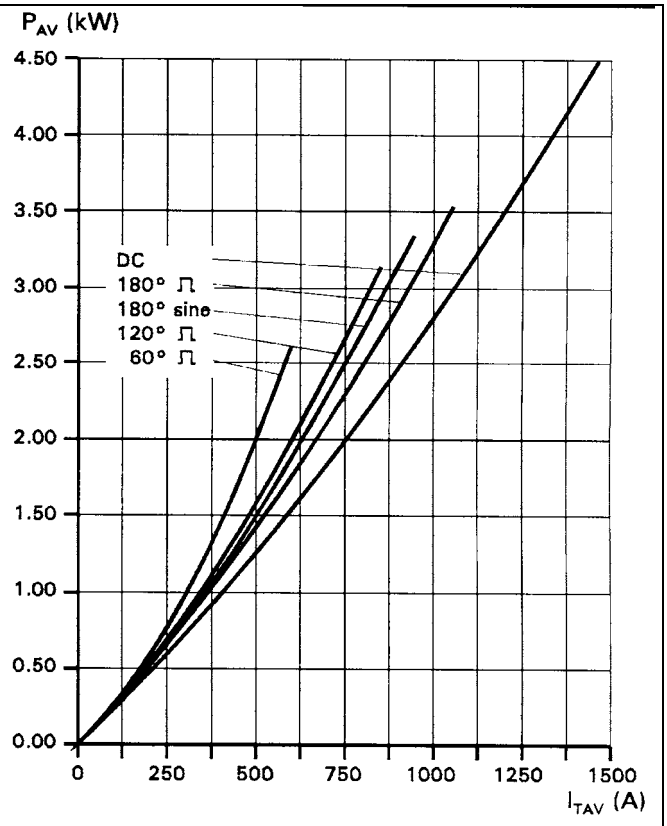

Fig. 8 Average on-state power dissipation vs. average on-state current. This figure corresponds to Fig. 3 of the 5SGA 30J4502 data sheet.

For some frequently encountered current waveforms, average on-state power dissipation is displayed in Fig. 8, as a function of average on-state current. The curves are based on the V_{TO} and r_T linear approximation, with V_{T0} and r_T at T_j = 125 °C. No turn-on or turn-off losses have been factored into Fig. 8; these must be calculated separately according to the application-specific conditions.

Fig. 9 specifies the surge current rating and corresponding fusing integral. The relationship between these two ratings was examined in the on-state parameter discussions, earlier in this section. The constraints linked to I_{TSM} and $\int i^2t$ that were mentioned there, also apply to Fig. 9.

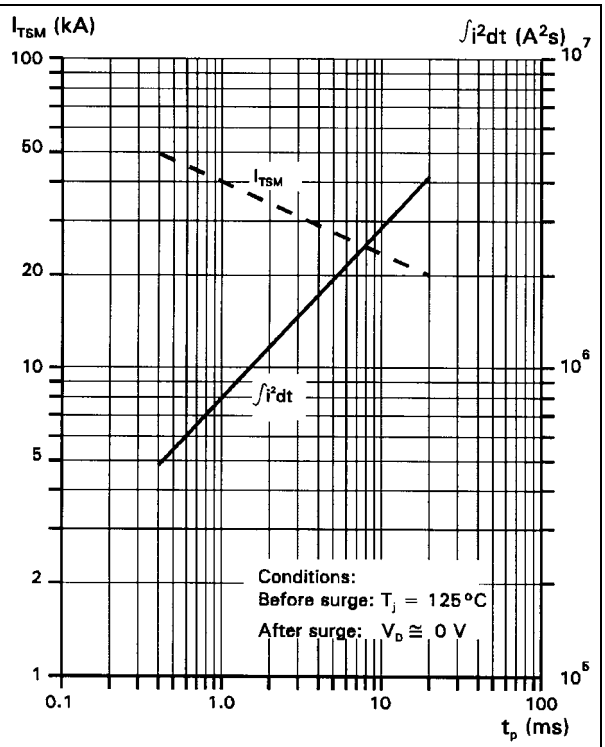

Fig. 9 Surge current and the fusing integral vs. pulse width. This figure corresponds to Fig. 4 of the 5SGA 30J4502 data sheet.

Blocking characteristics

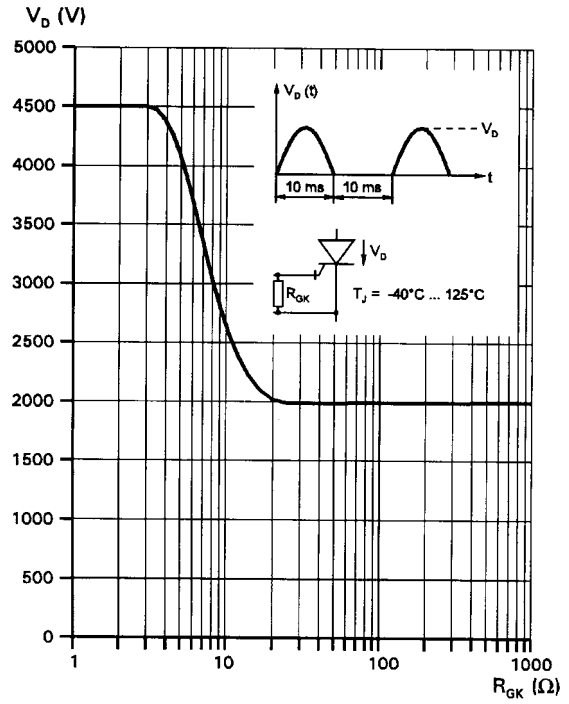

Fig. 10 Forward blocking voltage vs. gate-cathode resistance. This figure corresponds to Fig. 5 of the 5SGA 30J4502 data sheet.

Unlike conventional thyristors, that are able to block rated V_{DRM} with an open gate, GTOs require a negative gate voltage, or at least a low-impedance gate-to-cathode resistor, in order to block full voltage at maximum junction temperature. The reason for this is that GTOs have no cathode shorts. As a consequence, anode leakage current must be shunted from the p-base (gate contact) to the cathode terminal through a resistor, or a negative voltage source, to prevent the cathode emitter from injecting electrons which could trigger the GTO.
It can be seen from Fig. 10 that, for the 5SGA 30J4502, full rated voltage can be blocked with a resistor of up to 3.3 Ω, and that $V_{D\,max}$ is reduced to 2000 V for $R_{GK} \geq 22\ \Omega$. Obviously, $R_{GK} \geq 22\ \Omega$ behaves like an open gate.
Under ordinary operating conditions, GTOs are biased with a negative gate voltage of around -15V from the gate unit, during blocking intervals. Provision of an R_{GK} may, nonetheless, be desirable insurance, should the gate unit fail for any reason, leaving the GTO to block rated voltage until power is interrupted. Unfortunately, R_{GK} dissipates energy while negative gate voltage from the gate unit is present.

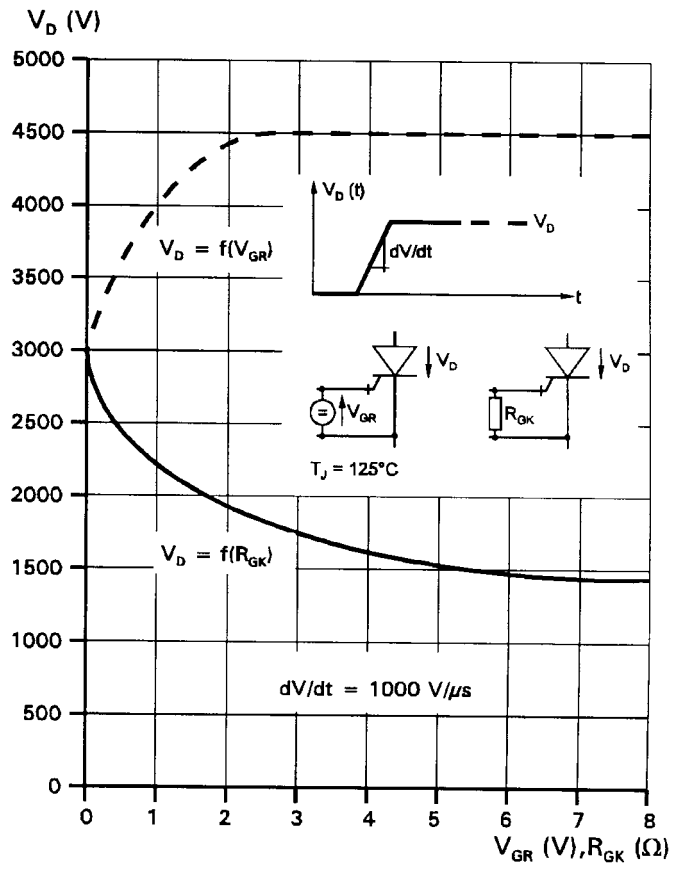

Fig. 11 Static dv/dt capability: Forward blocking voltage vs. negative gate voltage (dotted line) and gate-to-cathode resistance (solid line) with dv/dt = 1000 V/µs applied. This figure corresponds to Fig. 6 of the 5SGA 30J4502 data sheet.

For the reasons cited above, GTO blocking voltage may also have to be reduced when a static dv/dt is applied. In addition to leakage current, junction capacitance charging current must then be bypassed to the cathode terminal. It can be seen from Fig. 11 that, for the 5SGA 30J4502, a V_{GR} of $\geq$ 2.5 V is necessary to regain full blocking rating, with a dv/dt of 1000 V/µs. With but a gate-to-cathode resistor, $V_{D\,max}$ is reduced to 3000 V if R_{GK} = 0 Ω, and to 1400 V when R_{GK}= 8 Ω.

Gate characteristics

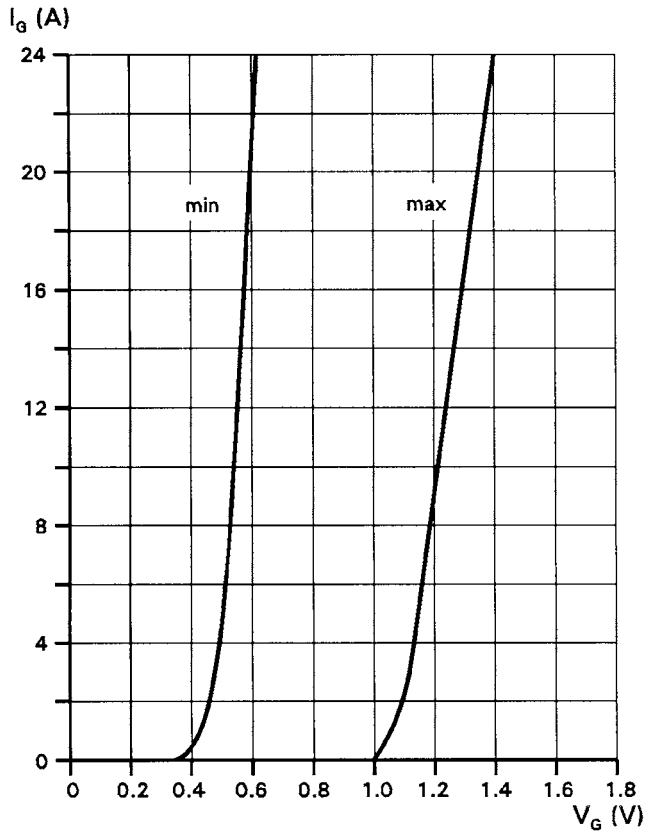

Fig. 12 Forward gate current vs. forward gate voltage. This figure corresponds to Fig. 7 of the 5SGA 30J4502 data sheet.

GTO forward gate characteristics are displayed in Fig. 12. The zone between the min. and max. curves reflects parameter variations between individual GTOs (production scattering), and allows for parameter shift over the specified temperature range. The characteristics are quasi-static, and valid for DC and low frequency AC gate currents. They do not define gate voltage when the GTO is turned on from high anode voltage, with high di/dt and di_G/dt; VG in this case is dynamic, and correspondingly much higher.

Generally, the gate-to-cathode impedance of a GTO is much lower than that of a conventional thyristor, for three main reasons:

1. A large number of individual GTO-segments are connected in parallel
2. GTOs do not have an amplifying gate, and the p-base conductivity is higher
3. The gate contact surface area is much greater

In conclusion, V_G is not an important parameter in standard GTO applications.

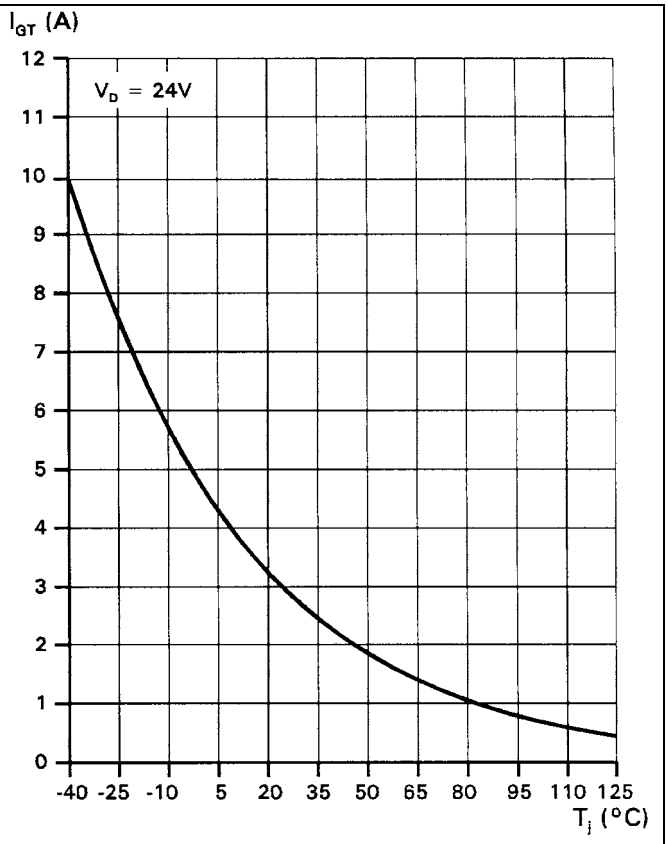

Fig. 13 Gate trigger current vs. junction temperature. This figure corresponds to Fig. 8 of the 5SGA 30J4502 data sheet.

Fig. 13 depicts the gate current necessary to trigger a GTO, with low anode voltage (V_D = 24 V). The gate trigger current specified here is the backporch current, to be furnished by the gate unit during on-state periods, in order to ensure that the GTO can take back load current from the freewheeling diode at any time. Backporch current is also required when anode current falls momentarily below the holding current. Note that specified I_{GT} is *not* sufficient to trigger the GTO from an elevated anode voltage, with high di/dt. In this case, a peak gate current (I_{GM}) in the range of (3...10) × I_{GT} at $T_{j(min)}$ is recommended to obtain good turn-on performance. The gate driver must also perform satisfactorily under worst case conditions of lowest expected junction temperature. In some cases, it may be advantageous to modulate the backporch current as a function of ambient temperature, since the worst case prevails only occasionally.

Turn-on characteristics

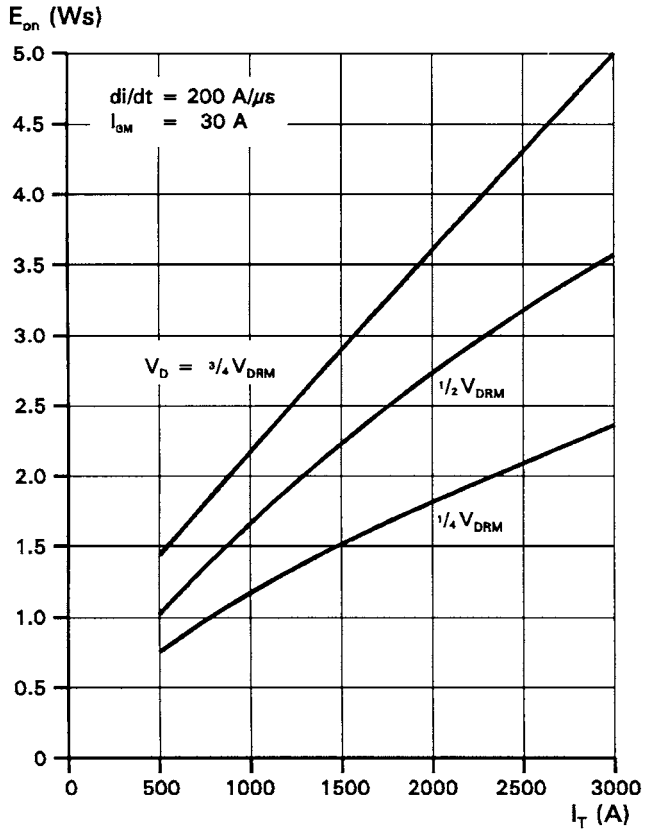

Fig. 14 Turn-on energy per pulse vs. on-state current and turn-on voltage. This figure corresponds to Fig. 9 of the 5SGA 30J4502 data sheet.

Fig. 14 shows E_{on} vs. I_T for 3 different anode voltages, with the same gate drive (I_{GM} = 30 A, di_G/dt = 20 A/µs).
Some of the test conditions common to all turn-on characteristics of a particular device are appended to Fig. 11. For the 5SGA 30J4502, these are:

di_G/dt = 20 A/µs
C_s = 6 µF
R_s = 5 Ω
T_j = 125 °C

It can be seen that the turn-on measurements are performed *with the RCD snubber discharge current included.*

Fig. 15 is similar to Fig. 14. The only difference is that V_D is kept constant (V_D = 0.5 V_{DRM}), and di/dt is varied between 100 and 300 A/µs. Therefore, the curve for ½ V_{DRM} on Fig. 14 is equivalent to the curve for 200 A/µs on Fig. 15.

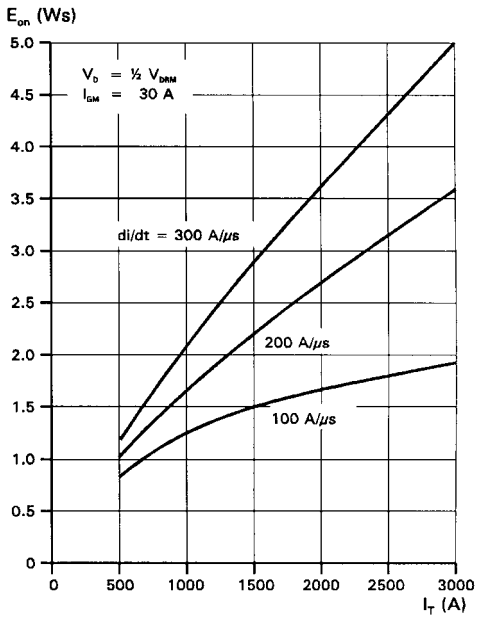

Fig. 15 Turn-on energy per pulse vs. on-state current and current rise rate. This figure corresponds to Fig. 10 of the 5SGA 30J4502 data sheet.

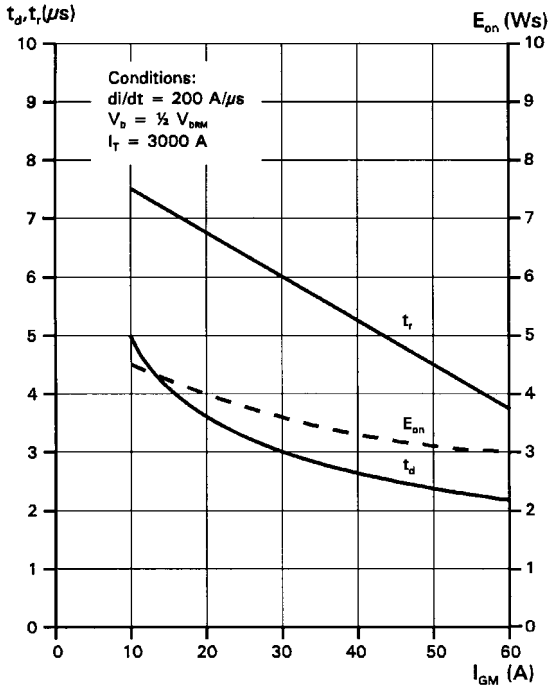

Fig. 16 Turn-on energy per pulse, delay time and rise time vs. peak gate current. This figure corresponds to Fig. 11 of the 5SGA 30J4502 data sheet.

Fig. 16 depicts the dependence of t_d, t_r, and E_{on}, on peak gate current, I_{GM}. As specified in the test conditions, these curves are valid for a gate current di_G/dt = 20 A/µs. It is clear that turn-on switching times and turn-on switching energy increase progressively with decreasing gate current. These dependencies become even more evident at higher anode di/dt's.

How to use Figs. 14 to 16.

By combining data presented in figs. 14 to 16, additional turn-on energy information can be obtained, under different conditions. Assuming that, as a first-order approximation, the trends portrayed do not vary for measurement conditions differing from those applicable to the graphs, E_{on} can be calculated for any combination of I_T, di/dt, V_D and I_{GM}.

Example:

Ascertain: E_{on} @ I_T = 2500 A, di/dt = 250 A/µs, V_D = ¾ V_{DRM} and I_{GM} = 60 A/µs.

From Fig. 14: E_{on1} @ 2500 A, ¾ V_{DRM} = 4.3 Ws.

From Fig. 15: @ 2500 A, the ratio f_2 = E_{on} (250* A/µs)/E_{on} (200 A/µs) = 3.7* Ws/3.2 Ws = 1.16

(obtained by linear interpolation between 200 and 300 A/µs).*

From Fig. 16: The ratio f_3 = E_{on} (60 A)/E_{on} (30 A) = 3.0 Ws/3.6 Ws = 0.83.

Result: E_{on} @ 2500 A, 250 A/µs, ¾ VDRM, 60 A ≈ $E_{on1} \cdot f_2 \cdot f_3$ = 4.3 Ws·1.16·0.83 = 4.1 Ws.

Although this type of calculation does not yield *exact* results (in reality, the trends shown do vary with changing conditions), it is useful as a *first-order approximation*. The accuracy is acceptable, as long as extrapolations are not made when conditions are quite different from standard conditions.
In the above example, note that the calculation shows how E_{on} can be reduced by increasing I_{GM}, despite an increase in di/dt from 200 to 250 A/µs.

Turn-off Characteristics

Typical turn-off waveforms are shown in Fig. 4. It can be seen that the negative gate current at turn-off rises *linearly* between zero and I_{GQ}. *This is the standard measurement condition for turn-off at ABB Semiconductors, for all standard GTOs*. The big advantage of the linear wave-shape is that it is exactly definable, thereby facilitating excellent reproducibility, even with different test equipments. However, in most applications, the gate current waveform at turn-off is more like an exponential, which mainly impacts on storage time and neg. peak gate current. For the same nominal di_{GQ}/dt, which is defined between 10 % and 50 % of I_{GQ} in the exponential case, t_s is higher and I_{GQ} is lower, for the exponential waveform.

No exhaustive correlation factors can be given, because the actual "exponential" waveform varies from case to case. ABB Semiconductors can provide assistance in evaluating the proper correlation factors for defined cases.

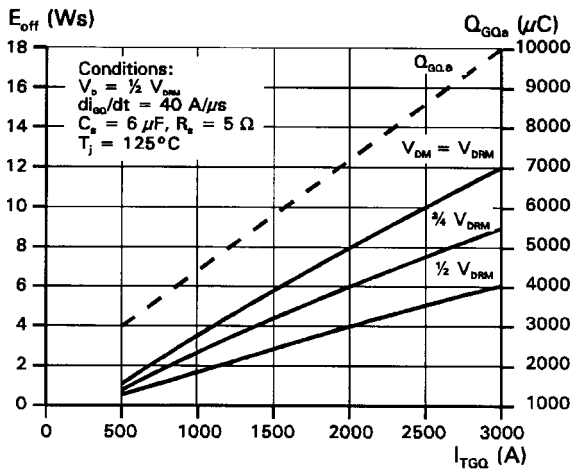

Fig. 17
Turn-off energy per pulse vs. turn-off current and peak turn-off voltage. Extracted gate charge vs. turn-off current.
This figure corresponds to Fig. 12 of the 5SGA 30J4502 data sheet.

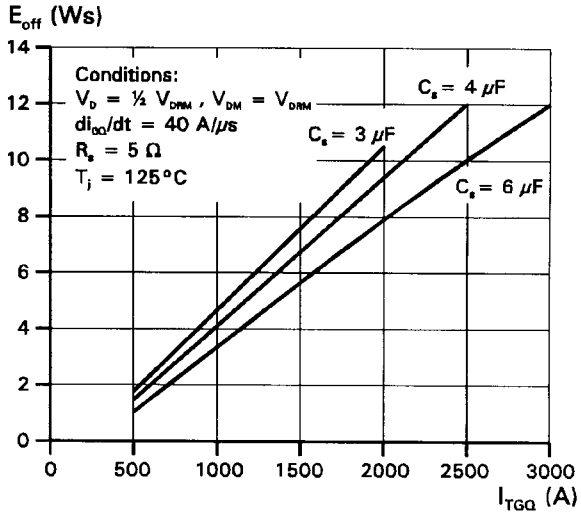

Fig. 18
Turn-off energy per pulse vs. turn-off current and snubber capacitance.
This figure corresponds to Fig. 13 of the 5SGA 30J4502 data sheet.

Figs. 17 and 18 show the relationship between E_{off} and I_{TGQ} for different values of V_{DM} (Fig. 17) and C_s (Fig. 18). Fig. 17 additionally specifies Q_{GQa}, which, according to Fig. 4, is the gate charge extracted during the storage time. Because Q_{GQb} is dependent on the driving voltage for the negative gate current (i.e. gate-unit specific), no general value for $Q_{GQ} = Q_{GQa} + Q_{GQb}$ can be specified. As a rule-of-thumb, $Q_{GQ} \approx 2 \cdot Q_{GQa}$ is a first-order approximation.

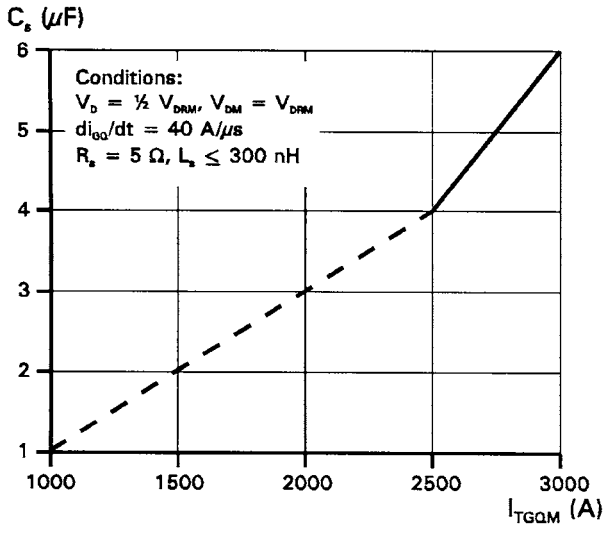

Fig. 19

Required snubber capacitor vs. max. allowable turn-off current.
This figure corresponds to Fig. 14 of the 5SGA 30J4502 data sheet.

The required snubber capacitor for a given turn-off current is specified in Fig. 19. The solid line specifies the current range where the GTO typically operates, and the dashed line is an extrapolation for low turn-off currents down to 1000 A. The turn-off safety margin can be considerably increased when the snubber stray inductance, L_s, is less than the 300 nH for which Fig. 19 applies. L_s = 200 nH is typical for today's converter designs and values as low as 100 nH can be achieved.
A major reduction in C_s can be realized with a "hard driven" GTO, i.e. a Gate Commutated Thyristor (GCT), as later in this section.

Fig. 20

Turn-off energy per pulse, storage time and peak turn-off gate current vs. junction temperature. This figure corresponds to Fig. 15 of the 5SGA 30J4502 data sheet.

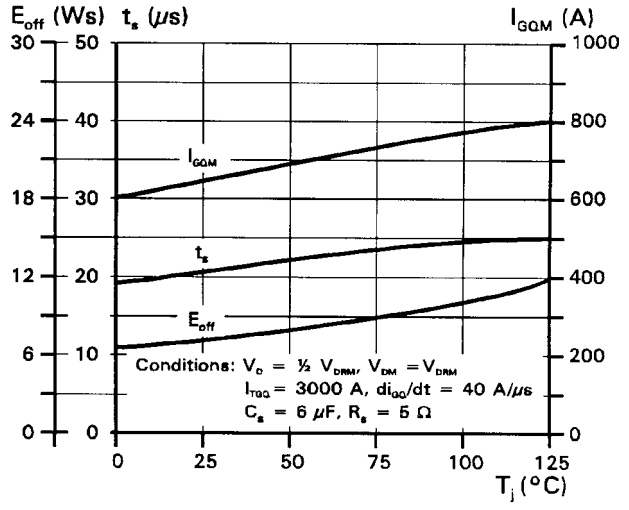

Fig. 20 shows the temperature dependence of E_{off}, t_s, and I_{GQM}. It is evident that, of these characteristics, E_{off} shows the greatest variation with T_j. Its value at 125 °C is approximately twice that at 0 °C.

Fig. 21

Storage time and peak turn-off gate current vs. neg. gate current rise rate. This figure corresponds to Fig. 16 of the 5SGA 30J4502 data sheet.

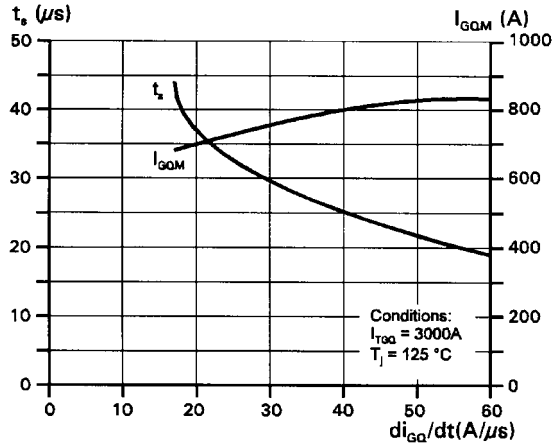

Fig. 21 shows that storage time increases progressively as di_{GQ}/dt is reduced. To ensure safe turn-off, it is highly recommended to avoid di_{GQ}/dt's below 20 A/µs for all GTOs. The storage time decreases much more with high di_{GQ}/dt than peak turn-off gate current increases.

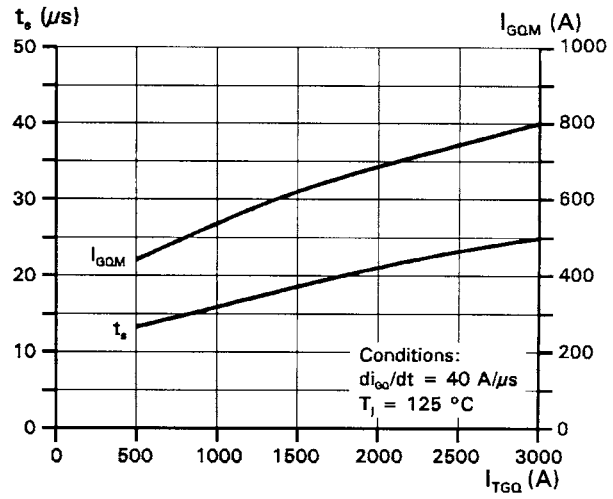

Fig. 22 Storage time and peak turn-off gate current vs. turn-off current. This figure corresponds to Fig. 17 of the 5SGA 30J4502 data sheet.

Fig. 22 shows the increase of I_{GQM} and t_s with higher turn-off current I_{TGQ}. It can be seen that the turn-off gain (the ratio I_{TGQ}/I_{GQM}) is close to unity at I_{TGQ} = 500 A, and approx. 3.8 at 3000 A. With an "exponential" neg. gate current, the turn-off gain would be somewhat higher.

Reverse Avalanche Capability

During operation with an antiparallel freewheeling diode, GTO reverse voltage, V_R, may exceed the rated value, V_{RRM}, due to stray inductance and the diode's forward recovery voltage spike at high di/dt. The GTO is then driven into reverse avalanche. This condition is not dangerous for the GTO, provided avalanche time and current are below 10 µs and 1000 A, respectively. However, the gate voltage must remain negative during this time (recommendation: V_{GR} = 10 V ... 15 V).
The above warning is reproduced from the last page of the data sheet of the 5SGA 30J4502. Additional information on this subject follows:

Fig. 23 shows a typical situation, where GTO_1 is connected to an antiparallel free-wheeling diode D_1. Here, both GTO_1 and D_1 form the upper switch of an inverter phase leg, with the lower GTO_2 carrying load current. GTO_2 is then turned off. The load current subsequently commutates from GTO_2 and its snubber circuit into D_1, with a di/dt determined by the DC link voltage and di/dt reactor. An inductive voltage, $V_{L\sigma} = L_\sigma \cdot di/dt$, plus the dynamic turn-on voltage V_{fr} associated with D_1, appears in the reverse direction across GTO_1. Assume now that each GTO is a conventional anode shorted type, connected to a standard gate unit. Inside the GTO, there is only one pn-junction able to block reverse voltage, the pn^+-junction on the cathode side. This junction, in fact, consists of thousands of parallel connected diodes (D_3) with a common anode, the p-base.

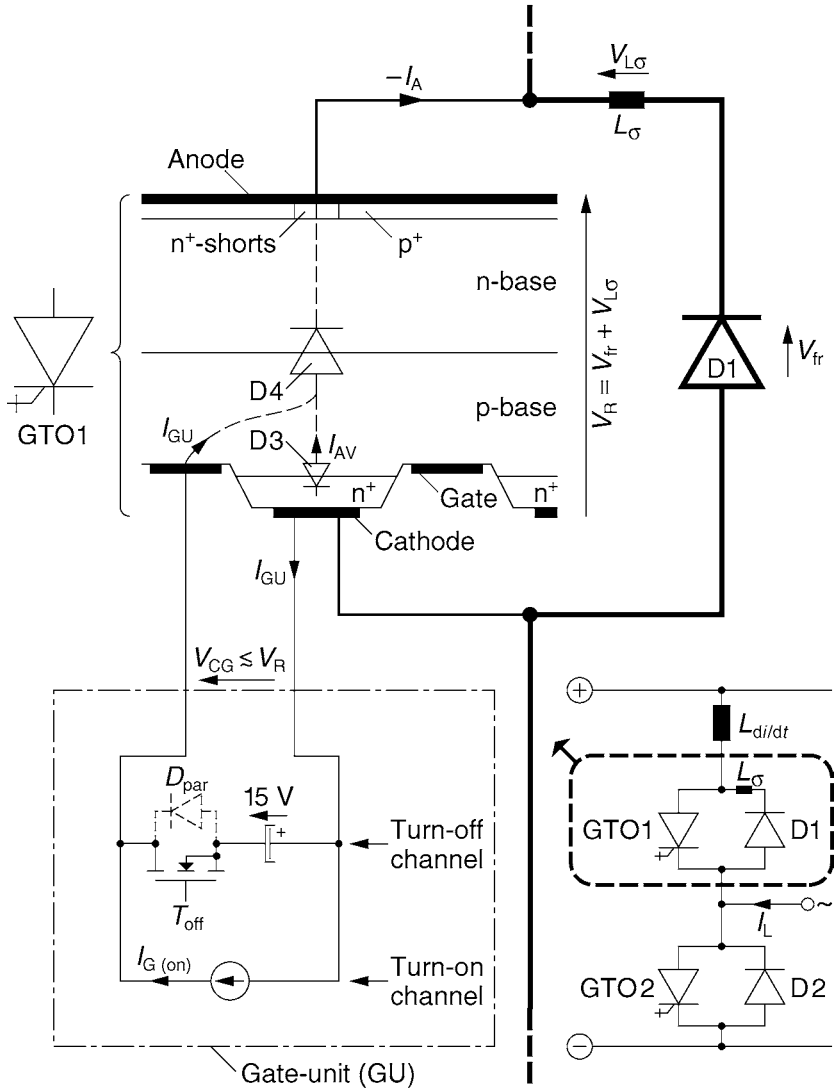

Fig. 23 GTO subjected to (transient) reverse overvoltage, caused by inductive voltage across L_σ and V_{fr} of antiparallel free-wheeling diode. Depending on design and status of the gate unit, a more or less significant current I_{GU} flows via gate unit from cathode to gate. If V_R exceeds the avalanche voltage of the gate-to-cathode junction D_3, this one acts as a clamping diode and absorbs the excessive current I_{AV}. This case must be considered when a GTO gate unit is designed and tested.

Almost the entire reverse voltage, V_R, appears across the gate and cathode terminals, with the negative polarity at the gate.

We have now to distinguish between two cases:-

1. V_R is lower than the avalanche voltage of D_3 (V_{av} = 20-25 V, typically).

   No current will flow through D_3, so there is no danger for the GTO. Instead, a stiff voltage (V_R) is applied across the terminals of the gate unit. The reaction of the gate unit now depends on its internal design and operating mode (turn-on, on-state, or off-state). In reality, it is probable that the unwanted negative gate voltage will

generate high currents and/or overvoltages in the turn-on and turn-off channels within the gate unit, which may be dangerous if the unit had not been designed for this operating condition.

2. V_R is bigger than V_{av}

   The situation is basically the same for the gate unit. V_{av} is the maximum voltage than can appear across the gate and cathode terminals, since the reverse biased diode D_3 acts as a clamp. The external circuit now determines the current flowing through D_3, with $-I_A = (I_{GU} + I_{AV})$, this being the GTO`s (negative) anode current.

For state-of-the-art converter designs, where the free-wheeling diode is located close to the GTO, and exhibits average V_{fr} voltages, ABB Semiconductors' GTOs are able to handle the reverse voltages without problems. If designed for this case, the gate unit does not suffer either. Care must be taken, however, in processing the gate unit feedback signal, if indeed it is still valid; it may in fact be temporarily distorted by the impressed negative gate voltage. Appropriate filtering may be necessary to circumvent this problem.

Guide to the Data Sheet of a GCT

A **GCT** (**G**ate-**C**ommutated **T**hyristor) consists of a conventional GTO wafer encapsulated in a special ceramic presspack housing with very low gate-to-cathode inductance. Such a device is driven by a special gate unit (GU), which also features a very low gate-to-cathode stray inductance. The combination of a GCT and its GU, is called an **IGCT** (**I**ntegrated **G**ate-**C**ommutated **T**hyristor), sometimes also referred to as a HD-GTO (**H**ard-**D**riven **GTO**).

Since the gate-to-cathode stray inductance (in the order of 5 nH) is about 1 % of the corresponding value of a conventional gate drive, the di_{GQ}/dt at turn-off is up to two orders of magnitude higher than for a conventionally driven GTO. This results in an extremely low storage time, combined with a very homogeneous and safe turn-off process, which even permits turn-off without a dv/dt-limiting snubber. The extremely low gate inductance also allows fast and high energy turn-on gate pulses, with correspondingly low IGCT turn-on times, t_d and t_r.

These properties make the GCT an ideal device for future high current, high voltage switching. The devices can also be connected in series, without costly selection of switching parameters, like delay and storage times.

The data sheet of a GCT, type 5SGY 35L4502, will now be examined, with respect to *GCT-specific ratings and characteristics.*

Features

- *Very low inductance gate connection*

As already described, a very low gate-to-cathode stray inductance is the major improvement, compared to a conventional GTO. It is achieved by a special design of ceramic presspack housing.

- *Transparent emitter buffer layer technology*

The transparent emitter buffer layer technology is fully described in Section 2. It allows a reduction in device thickness (and therefore V_T), without compromising dynamic performance. It transpires that this technology is best, when incorporated into a hard drive GCT.

Other features are similar to those described for the conventional GTO, at the beginning of this section.

Blocking

Since the silicon wafer is the same as in a conventional GTO, there is no difference in blocking behaviour, or in the relevant specifications.

Mechanical data

There is no basic difference to a conventional GTO, with respect to mechanical data.

Presspack housing

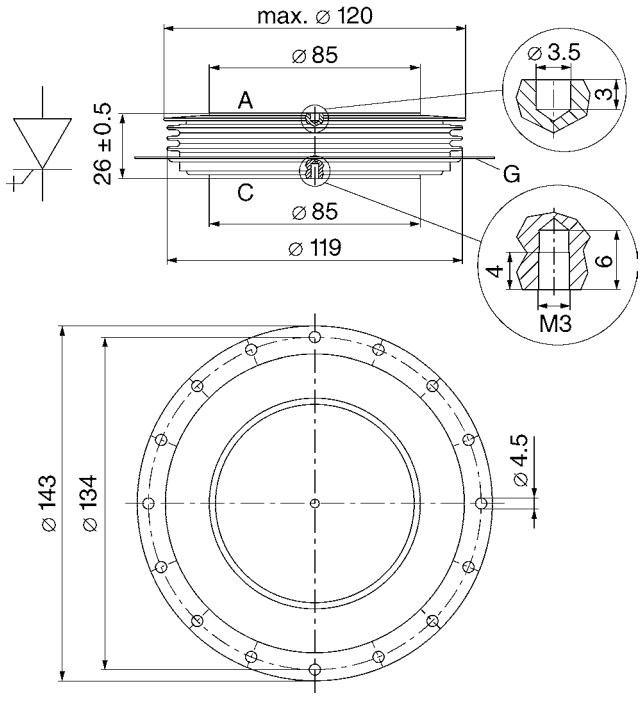

Fig. 24 Outline drawing of the press-pack housing for the 5SGY 35L4502. All dimensions are nominal values in millimetres unless stated otherwise.

By its nature, the housing of the GCT differs from the GTO mainly with respect to the gate connection. The faston connectors and coaxial gate lead are replaced by a concentric metal disc which is fed through the ceramic wall along the whole circumference and is somewhat reminiscent of a flying saucer!
Fig. 25 illustrates the way a coaxial GCT is mounted in its low-inductance gate unit:

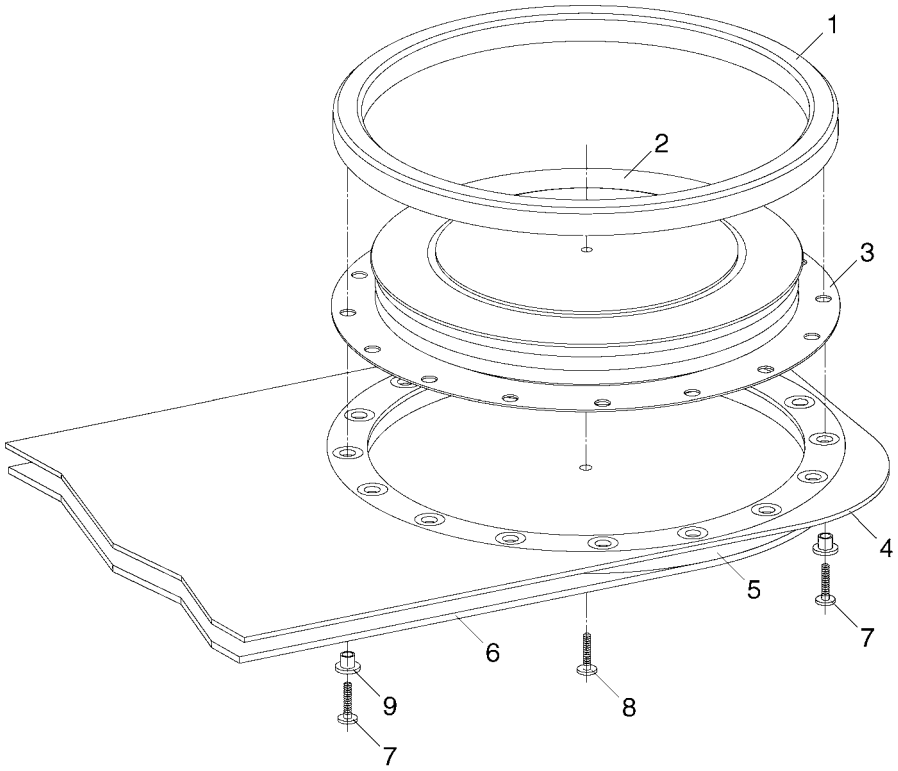

Fig. 25 Connection of GCT to gate unit

1. mounting collar with threaded holes (M3)
2. GCT
3. Gate flange with ∅ 4.5 mm through holes
4. Double-layer PCB for gate and aux. cathode connection
5. Metal spacing ring with ∅ 4.5 mm through holes
6. Gate-unit support plate (at cathode potential)
7. Gate connection screws (M3)
8. Central retaining screw (M3)
9. Insulation ferrules

The heart of the low-inductance connection is the double-layer PCB. The upper surface connects gate flange of the GCT and the bottom PCB surface connects to the GCT cathode which in turn contacts the gate driver support plate (6) via the spacing ring (5). Inductance between gate-unit and GCT is minimal because of the “strip-line” PCB connection.

The GCT is located in its driver and held in place by the gate flange mounting collar (1) and its 16 M3 screws. A central M3 screw (8) holds the device against the support plate (6) and prevents movement of the device during shipment (which might otherwise fatigue the bellowed gate flange).

On-state

This is presented in the same way as for a conventional GTO except that on-state voltages are much lower due to the buffer-layer technology.

Gate

This is similar to a conventional GTO except that the gate trigger current I_{GT} is very much lower as a result of the transparent emitter technology.

Turn-on

The turn-on switching parameters are defined under conventional gate drive conditions, hence the values are similar to those of a conventional GTO. Both, the switching times and the turn-on energy are drastically reduced if the GCT is turned on "hard", i.e. with a high di_G/dt and I_{GM} both of which are easily achieved thanks to the low inductance construction. The maximum allowable di/dt then increases considerably.

Turn-off (snubbered)

The turn-off parameters naturally differ most to a conventionally driven GTO. Since a GCT can basically be driven with a snubber or snubberlessly, the turn-off parameters are given for both modes.
It can be seen that the GCT is turned off with an extremely high di_{GQ}/dt of 3500 A/µs. In the first table, the device is snubbered with 4 µF, hence the max. turn-off current is very high and the turn-off switching energy comparatively. It should be noted that the peak turn-off gate current is the same as the anode current being switched off, i.e. the turn-off gain is 1, compared to approx. 4 for a conventional GTO. On the other hand, the duration of the gate pulse is extremely low (ts ≈ 2 µs), so the extracted gate charge is actually lower than for a conventional GTO.

Turn-off switching (snubberless)

Without snubber, the max. controllable turn-off current is lower, and the max. junction temp. is limited to 115 °C. "V_{DSP} = 4000 V" means that there is no classical spike as known from the snubbered operation; instead, the voltage rises up to its maximum (V_{DM}) without local minima or maxima in-between. On the last page of the GCT data sheet, both the waveforms for snubbered and snubberless operation are displayed.
If the same anode current is switched off, the turn-off energy *in the GCT* is lower with a snubber than without. However, since the snubber itself produces losses, the *total* switching losses are lower in the snubberless operation.

Thermal

For snubberless switching, the maximum junction temperature is restricted to T_{j1} = 115 °C, whereas for the operation with a snubber, T_{j2} is limited to 125 °C, as for GTOs.
The thermal resistance of a GCT is that of a GTO of the same size. Although the low-inductance gate contact feeds are embedded in the copper pole piece on the cathode side, slightly reducing the thermal

conductivity, but both calculations and measurements have shown that the effect on R_{thJC} is negligible.

Characteristics

Basically, the presentation of characteristics for a GCT are the same as for a GTO, so no particular explanations are required. Most parameters (e.g. blocking, thermal, on-state, gate, and turn-on) differ slightly or not at all from those of GTOs, whereas the turn-off data differs considerably. This enhanced turn-off capability is the key to a number of new applications not previously accessible to GTOs. See Section 5 for more details.

3.2 Fast Recovery Diodes

Introduction

In Section 3.1, a typical GTO data sheet was dissected in great detail to facilitate understanding of how the device works, how it is rated and characterized, and how this data is presented to the device user. If this exercise were to be repeated “as is” for a fast recovery diode, much repetition would be unavoidable, given that in many respects (on-state, mechanical, and thermal properties for instance), diodes and GTOs are rather similar. For this reason, only *diode-specific issues* will be addressed in this section, namely *turn-on* and *turn-off* characteristics. Because the turn-off conditions for a *free-wheeling* diode are rather different from those of a *snubber* diode, a distinction between these two types will be made.
The free-wheeling diode data sheet is explained by means of the 5SDF 13H4501 and the snubber diode data sheet by the 5SDF 03D4501.

Turn-on Characteristic of a Diode

The turn-on behaviour of a diode will be explained by means of the 5SDF 13H4501 free-wheeling type. In that the physical processes within a diode during turn-on are basically the same for all types, the following statements are qualitatively true for snubber diodes as well. Fig. 26 shows the initial forward voltage overshoot (often referred to as *dynamic forward voltage* or *forward recovery voltage*), when the diode turns on with a high di/dt. V_{fr} (**f**orward **r**ecovery **v**oltage) is the peak voltage, and t_{fr} characterises the decay of the overshoot.
The voltage overshoot originates from the fact that conductivity of the diode is initially reduced, because the number of free charge carriers available is much lower than in the steady-state. The device needs time to build up the required electron and hole concentration, within the bulk of the silicon. Measurements have shown that the V_{fr} vs. di/dt characteristic is fairly linear, or slightly digressive. V_{fr} values at 125 °C are about double those at 25 °C. This behaviour can be explained by reduced charge carrier mobility at elevated temperatures.
Scatter in V_{fr}, due to process variations between units of the same design, is very small.

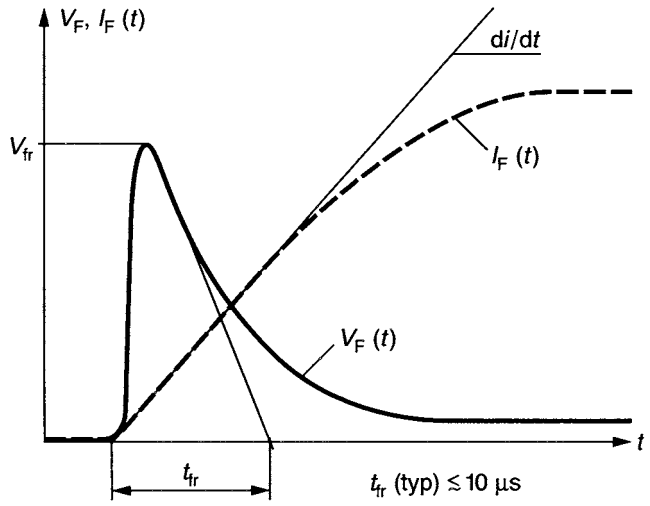

Fig. 26 Typical forward voltage waveform when the diode is turned on with high di/dt. This figure corresponds to Fig. 4 of the 5SDF 13H4501 data sheet.

Comparing V_{fr} values between diodes of the same area but different thickness, it is striking that dynamic forward voltage increases somewhat exponentially with device thickness. This is explicable by the difficulty in achieving steady-state carrier concentration in a thick device within a few µs.

Meaning of V_{fr} for a free-wheeling diode

It was explained in paragraph 3.1 (GTO Reverse Avalanche Capability), that the dynamic forward voltage of the free-wheeling diode appears as a reverse voltage across the GTO during current commutation. In order to avoid problems with the GTO gate unit and the GTO itself, V_{fr} should be as low as possible.
The dynamic forward voltage also produces turn-on losses. Their order of magnitude will be estimated for the 5SDF 13H4501. At di/dt = 500 A/µs, T_j = 125 °C, V_{fr} = 50 V (see Fig. 27 below), and t_{fr} = 5 µs (assumption):

$$E_{on} \approx \frac{1}{6} 50V \cdot (500A/\mu s \cdot 5\mu s) \cdot 5\mu s = 0.1J$$

Compared to expected turn-off losses of approximately 1.5 J under the same operating conditions, the turn-on losses are small and can be neglected. However, they will not be negligible when considerably higher di/dt's have to be switched with high-voltage diodes, ≥6 kV.
In the 5SDF 13H4501 data sheet, V_{fr} vs. di/dt is characterised by the following figure:

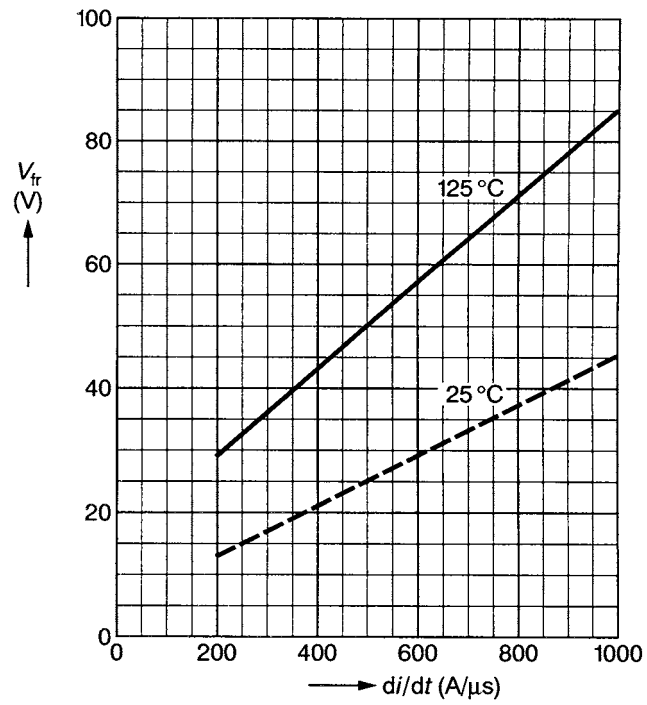

Fig. 27 Forward recovery voltage vs. turn-on di/dt (max. values). This figure corresponds to Fig. 5 of the 5SDF 13H4501 data sheet.

Meaning of V_{fr} for a Snubber Diode

The snubber diode for a GTO, often, although not exclusively, turns on with the same di/dt as the GTO turns off, typically at several kA/µs. The sum of the dynamic forward voltage across the snubber diode, plus the inductive voltage across the snubber stray inductance, plus the capacitive voltage of the snubber capacitor impress a *spike voltage* across the GTO, which can reduce the GTO`s turn-off capability if too high.
Turn-on losses, thanks to the high di/dt, most likely are greater than for a free-wheeling diode. On the other hand, losses are generally not a critical issue for a snubber diode. They will probably have to be reckoned with, however, in future high-voltage, high-frequency, applications. The data sheets will then have to include E_{on} data.
In the 5SDF 03D4501 data sheet, V_{fr} vs. di/dt is characterised by the following figure:

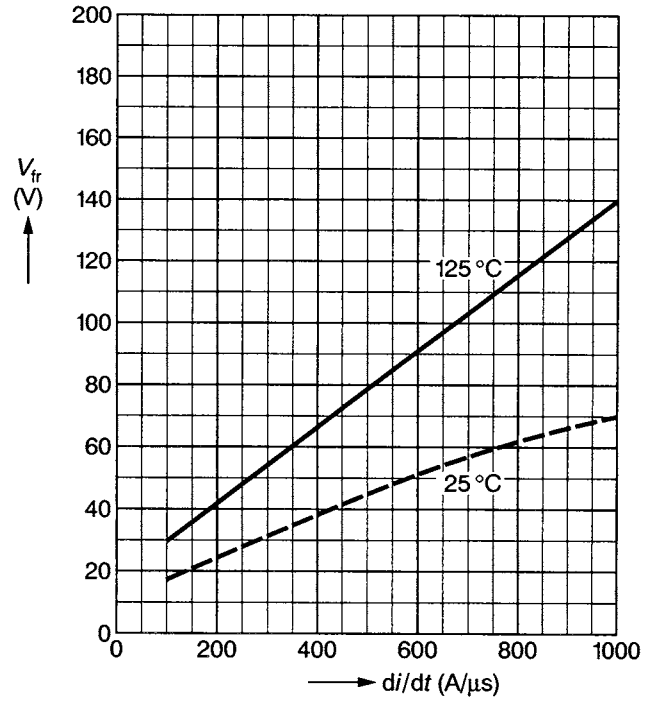

Fig. 28 Forward recovery voltage vs. turn-on di/dt (max. values). This figure corresponds to Fig. 5 of the 5SDF 03D4501 data sheet.

Turn-off Characteristics of a Free-Wheeling Diode

The turn-off characteristics of a free-wheeling diode are explained by means of figures 6-11 in the 5SDF 13H4501 data sheet (Figs. 29 - 34):
Fig. 29 depicts typical turn-off current and voltage waveforms for a free-wheeling diode, in conjunction with a "GTO-snubber". The forward current, I_F, is switched off with a certain di/dt (determined by the driving DC link voltage and the di/dt limiting inductance), and continues to flow in the reverse direction until the pn junction is once again able to block reverse voltage. At this time, the reverse recovery current has reached its peak value I_{rr}. The subsequent decay of the current and rise in reverse voltage are mainly determined by the diode itself (see Section 2), and the dv/dt-limiting snubber capacitor.

It is characteristic that, in a diode connected to a relatively large snubber capacitance, as a "GTO-snubber" normally is, the current first drops with a high di/dt, then terminates with a so-called tail current, often referred to as "rucksack". It is the goal of the diode design engineer to ensure that the tail current decays in a “soft” manner, that is without ringing or overshoot provoking “snap”, and that tail current and tail time are so small as to not contribute much to turn-off losses, despite reverse voltage being already high at this time.

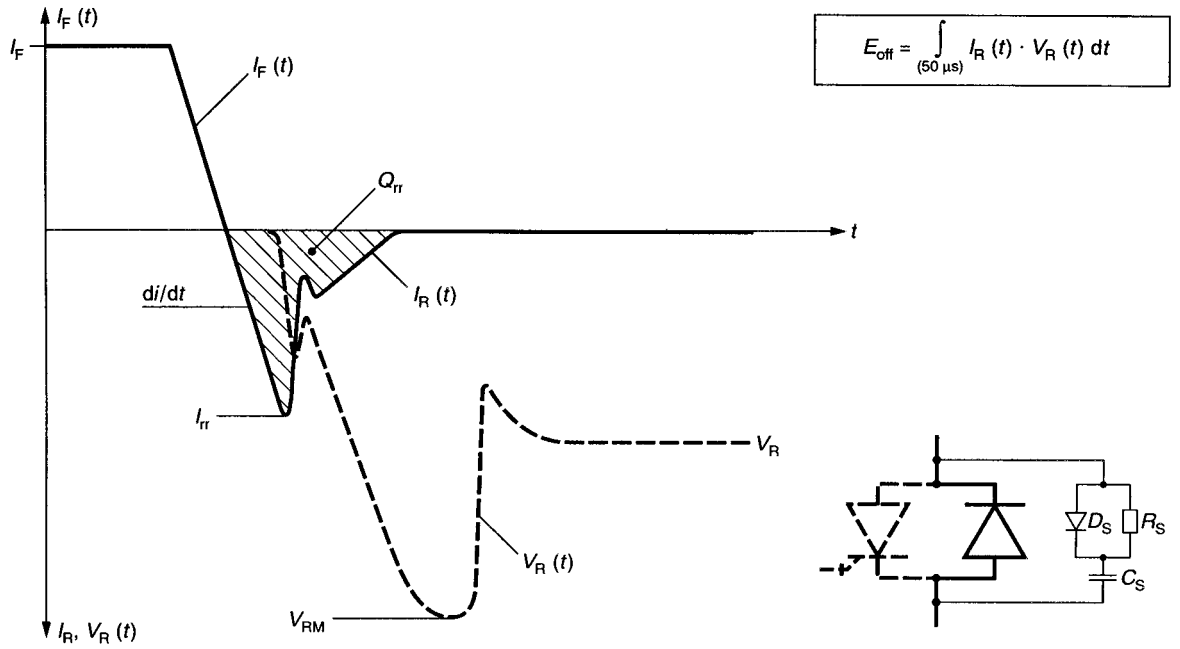

Fig. 29 Typical current and voltage waveforms of a free-wheeling diode, connected antiparallel to a GTO and its snubber circuit (e.g. type RCD).This figure corresponds to Fig. 6 of the 5SDF 13H4501 data sheet.

Together with demands for high blocking voltages and low on-state voltages, these dynamic requirements pose a real challenge, since most of them are contradictory. ABB Semiconductors is attempting to address these issues by evaluating and adopting new manufacturing processes, like electron or proton irradiation.

In many applications, more sophisticated snubber circuits like Undeland/Marquardt/McMurray etc., are used to reduce snubber power losses. In these cases, the voltage waveform differs from the one illustrated in Fig. 4, mainly with respect to the voltage overshoot, which is less than for an RCD snubber. However, the recovery characteristics of the diode remain virtually the same, because they are determined by the *voltage rise rate,* and not by the peak voltage. Therefore, all figures and curves in the data sheet are valid for most varieties of snubber circuits.

Figures 30 and 31 illustrate reverse recovery current and charge (see Fig. 29 for definition of Q_{rr}), as a function of commutating di/dt, for three different on-state currents I_F. Other relevant measurement conditions are listed in the boxes; it can be seen that the curves apply for a wide range of C_s and V_{RM}. At operating temperatures below 125 °C, the values of I_{rr} and Q_{rr} are correspondingly lower.

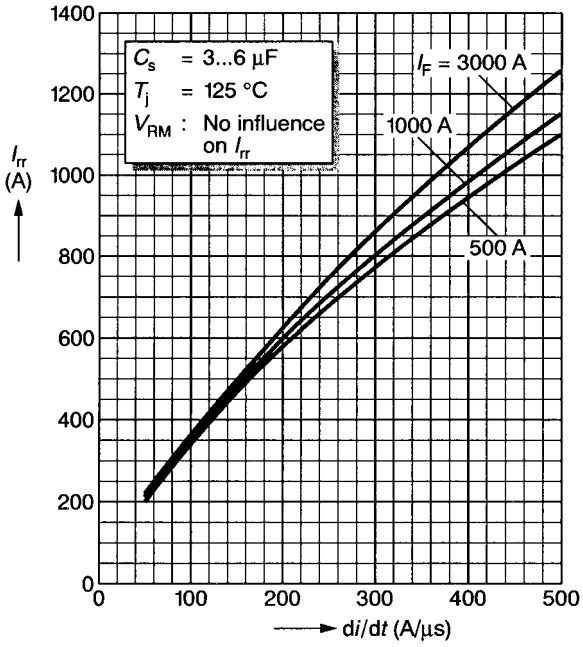

Fig. 30

Reverse recovery current vs. turn-off di/dt (max. values).

This figure corresponds to Fig. 7 of the 5SDF 13H4501 data sheet.

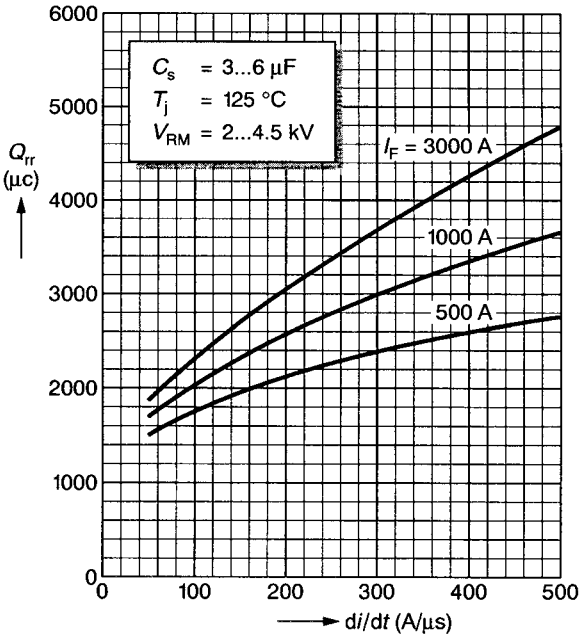

Fig. 31

Reverse recovery charge vs. turn-off di/dt (max. values).

This figure corresponds to Fig. 8 of the 5SDF 13H4501 data sheet.

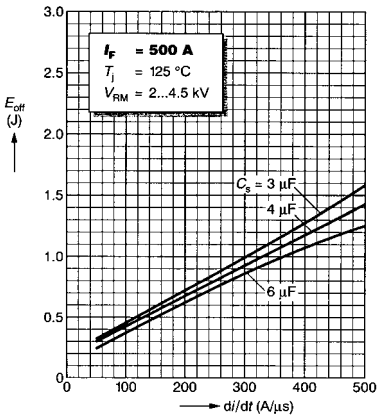

Fig. 32

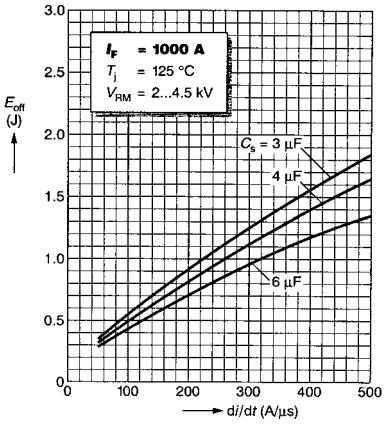

Fig. 33

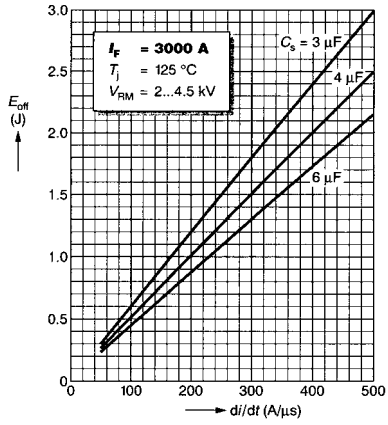

Fig. 34

Figs. 32, 33 and 34

Turn-off energy vs. turn-off di/dt for I_F = 500 A, 1000 A and 3000 A (max. values).

These figures correspond to Figs. 9 - 11 of the 5SDF 13H4501 data sheet.

Figs. 32 - 34 depict turn-off energy as a function of commutating di/dt, for three capacitor values, and three on-state currents. Again, the curves are valid over a wide range of peak voltages, V_{RM}. This may be explained by the fact that the reverse recovery current is nearly zero at V_R = 2 kV, for the 5SDF 13H4501 with the indicated conditions.
E_{off} is correspondingly lower at junction temperatures less than 125 °C.

Turn-off Characteristics of a Snubber Diode

The turn-off characteristics of a snubber diode are explained by means of Figs. 10 and 11 in the 5SDF 03D4501 data sheet. These figures describe the turn-off behaviour under classic turn-off conditions (linear di/dt and RC snubber):

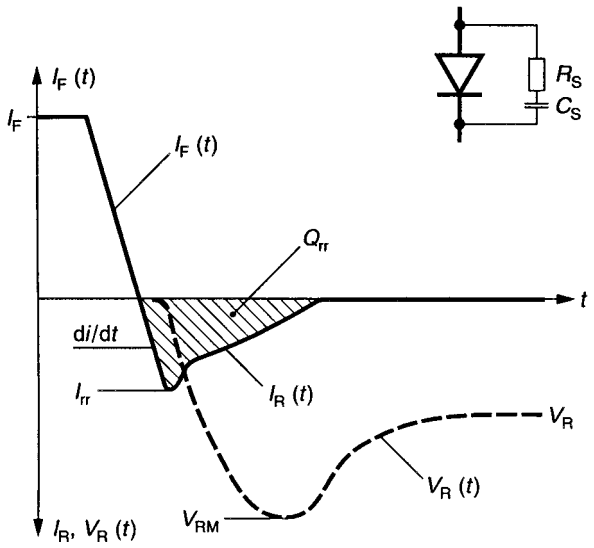

Fig. 35

Typical current and voltage waveforms of a fast recovery diode when turned off conventionally, i.e. with linear di/dt and RC snubber.

This figure corresponds to Fig. 6 of the 5SDF 03D4501 data sheet.

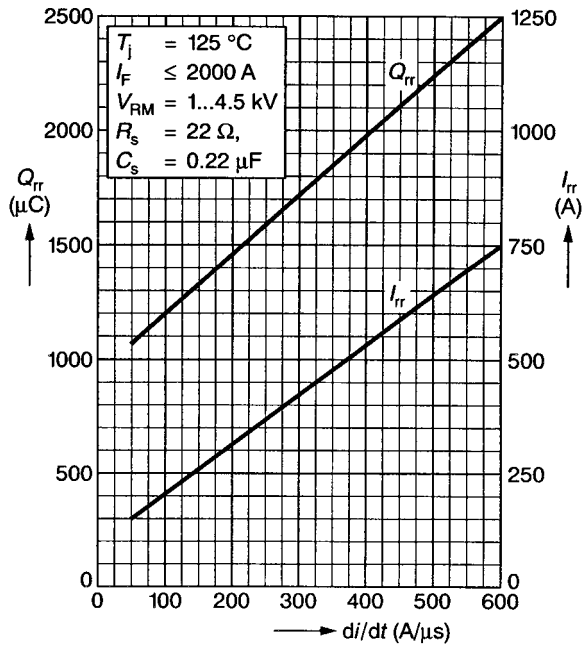

Fig. 36

Reverse recovery current and reverse recovery charge vs. turn-off di/dt for a fast recovery diode when conventionally switched off according to Fig. 35.

This figure corresponds to Fig. 7 of the 5SDF 03D4501 data sheet.

Fig. 35 depicts typical current and voltage waveforms, and serves to define the key parameters, I_{rr} and Q_{rr}, shown in Fig. 36 as a function of commutating di/dt with the conditions indicated.

Fig. 36 primarily serves to characterise the diode under standardised measurement conditions, as adopted by most diode manufacturers. This allows the converter design engineer to compare competitive products. However, it does not describe the behaviour of the device

when used in an Undeland/Marquardt or McMurray snubber circuit, since the relevant operating conditions at turn-off are totally different.

Turn-off of a snubber diode in an Undeland snubber circuit

Fig. 37 shows the well-known basic circuit of a GTO inverter; one phase leg with a so-called Undeland snubber circuit (often also referred to as Marquardt circuit) is shown in detail. Although the snubber circuit looks quite simple, its operation under the different circumstances is rather complicate, and a detailed description would exceed the scope of this book. The main principle can be summarised as follows: When GTO_1 turns off, C_S and D_{S1} act as dv/dt limiters. For GTO_2, C_S and C_{Cl} are in fact connected in series, i.e. the resulting snubber capacitance is slightly* lower than for GTO_1 (*in practice, $C_{Cl} \geq 5 \cdot C_S$). During operation, C_{Cl} is at DC voltage and gets a small amount of overvoltage whenever a GTO turns off, but this additional charge is fed back to the DC link capacitor via R_{Cl} between the turn-off events, thus regenerating part of the energy in C_{Cl}.

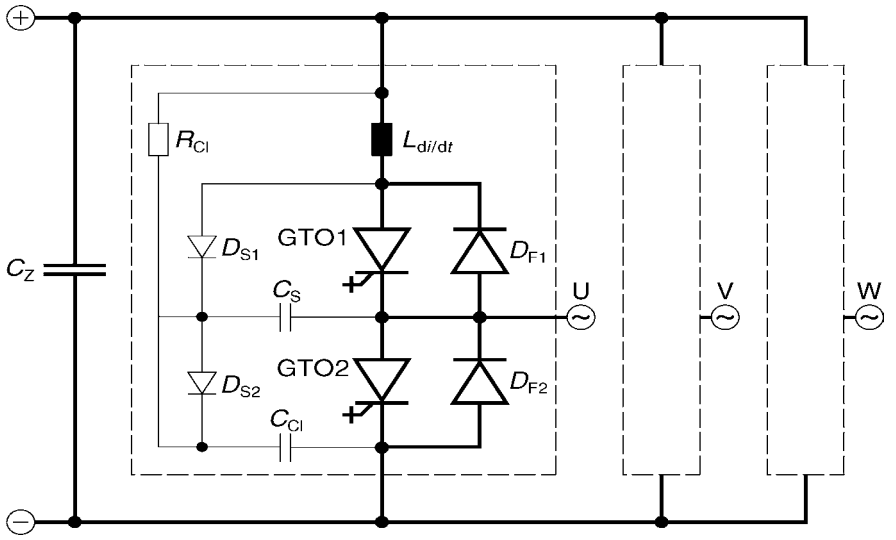

Fig. 37 Basic circuit of a GTO inverter, consisting of three phase-legs with an Undeland snubber.

Snubber components:
D_{S1}: "Upper" snubber diode
D_{S2}: "Lower" snubber diode
C_S: Snubber capacitor
C_{Cl}: Clamp capacitor
R_{Cl}: Clamp resistor

The circuit very effectively clamps the V_{DM} across the GTO (and, of course, the V_{RM} of the adjacent free-wheeling diode) and allows to regenerate part of the snubber energy; it is therefore widely used and very attractive in inverters with high DC link voltages.

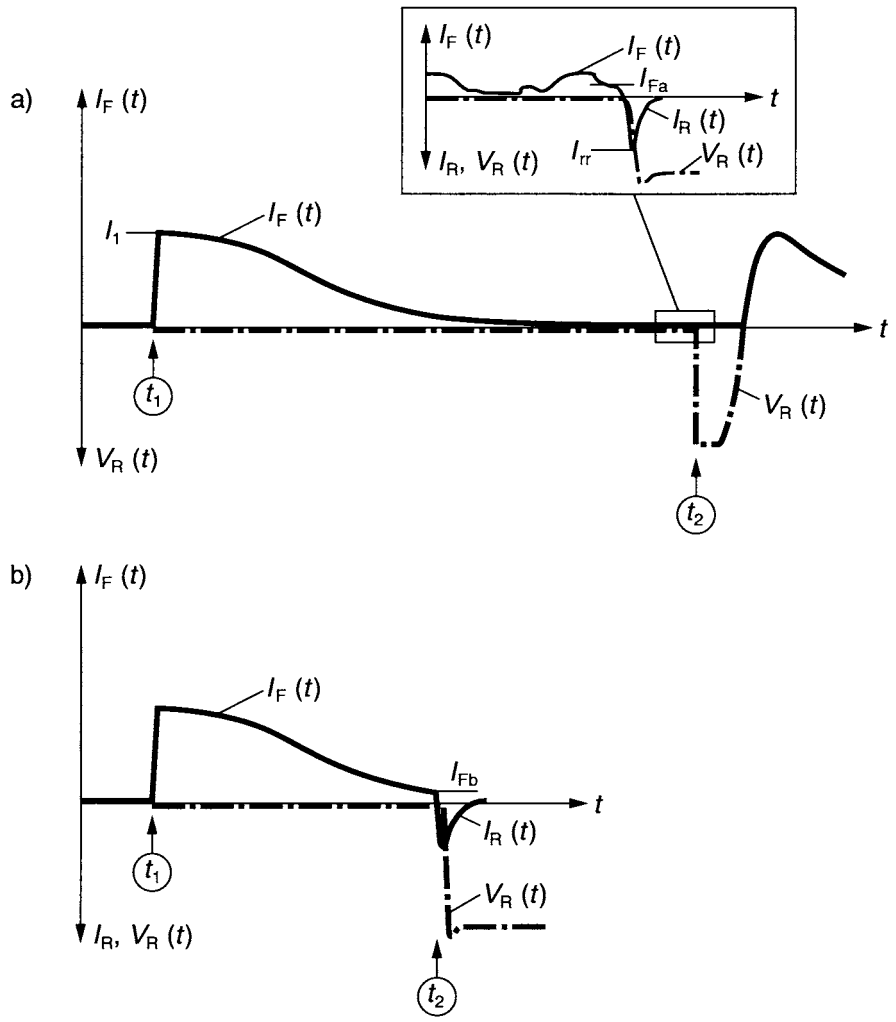

Fig. 38 Typical current and voltage waveforms of the upper snubber diode (D_{S1} in Fig. 37) and characteristic diode-turn-off events:

a) Turn-off due to DC voltage fluctuations

b) Turn-off due to short time interval between t_1 and t_2.

t_1: GTO_1 turns off; t_2: GTO_1 turns on (Fig. 37)

Note: The current and voltage waveforms for D_{S1} look different when GTO_2 is switched on and off or when the load current is close to zero.

The relevant voltage and current waveforms to discuss the turn-off behaviour of the diode are depicted in fig. 38. We consider the upper diode D_{S1}. It can be seen that, in fig. 38 a, the diode current slowly adapts to the time axis and is close to zero when the upper GTO_1 is turned on, i.e. no real turn-off stress is expected at the first moment. However, when we look more carefully to the diode forward current at the instant t_2, we can see that a somewhat arbitrary current $I_F(t)$ still flows in D_{S1}. It originates from the fact that the DC link voltage is not absolutely constant but varies due to several reasons.

As a consequence, C_S and C_{Cl} are continuously charged and discharged by relatively small currents, whereby the charging currents flow through the snubber diodes. When now GTO_1 turns on at t_2, D_{S1} is conducting a small current I_{Fa} (typically some amps or tens of amps), and the subsequent turn-off process causes a major dynamic stress to D_{S1}.

Fig. 38b shows a situation where GTO_1 is turned on at an instant when D_{S1} is still carrying a relatively high current I_{Fb} of typically more than 100 A. Except that the two currents I_{Fa} and I_{Fb} may be different in their respective amplitudes, both cases basically mean the same stress for the snubber diode, as discussed in the following.

We consider the loop GTO_1 - D_{S1} - C_S. Because it is a snubber, the loop inductance is very low (typically 100 - 300 nH). When GTO_1 turns on, the difference between the DC link voltage and the GTO anode voltage is applied across the snubber stray inductance, and the diode current is switched off by a di/dt of several 100 or even more than 1000 A/µs. This "hard" commutation yields a diode reverse recovery current which exceeds the previous forward current by far. After D_{S1} is able to block reverse voltage, the voltage of C_S (which is approximately the DC link voltage) is applied across the snubber diode with a very high dv/dt which is only limited by the finite turn-on velocity of the GTO and the junction capacitance of the diode (note that the snubber diode itself has no snubber at all in the considered case!)

Therefore, a high reverse current appears simultaneously with a high reverse voltage and causes a tremendous instantaneous power loss. Moreover, when the diode is switched off from a low forward current in the range of 10 - 150 A, the charge carrier concentration is low and not homogeneously distributed over the entire wafer area, hence there is a risk that the diode reverse current snaps off and begins to oscillate.

ABB Semiconductors has recognised at an early stage that these new requirements call for a special design of a snubber diode. This understanding was underlined by a series of tests which clearly showed that the design and manufacturing processes of conventional (free-wheeling) fast recovery diodes were no more applicable in the same way for modern high-voltage snubber diodes. Therefore, design and processes have been optimised in order to the meet these new requirements, and major investments have been made for qualification and production test equipment. Even in RCD snubber configurations, the snubber diode may be exposed to hard turn-off conditions as just described above (case a).

By connecting an RC-snubber in parallel to the snubber diode, the stress across the diode would be reduced, but both the GTO voltage fall time (and hence GTO turn-on stress) and turn-on losses would be increased. That is why most users prefer diodes that are robust enough to operate without snubber even under worst case conditions. The 5SDF 03D4501 is qualified for DC link voltages up to 3.2 kV without snubber.

Quality assurance for the new generation of snubber diodes from ABB Semiconductors

Since the measurement with a linear di/dt in the order of 100-300 A/µs just serves to compare diodes with other types, but is no more suited to characterise them under modern application conditions, ABB Semiconductors has introduced a routine test (performed at final inspection) which exactly reflects the conditions discussed above.

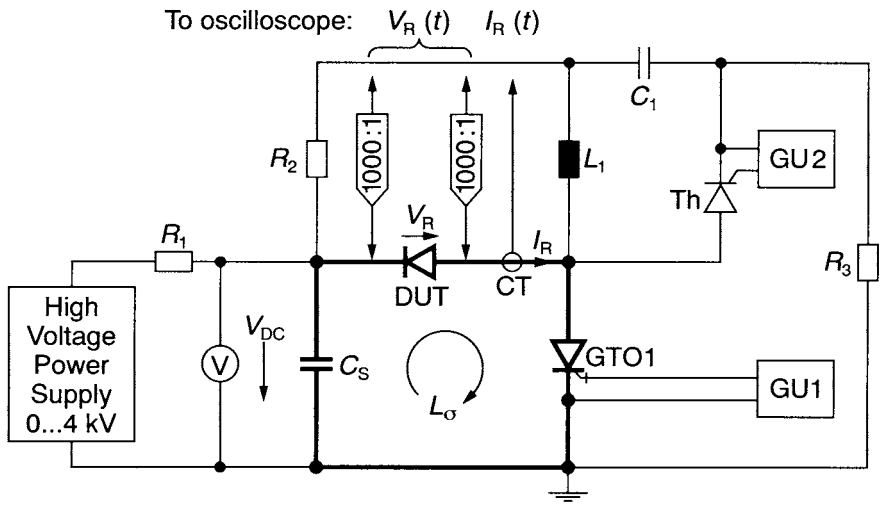

Fig. 39 Test circuit to evaluate the behaviour of snubber diodes under worst case conditions.

The commutation loop is drawn in **bold**

DUT: Diode under test (clamped in a heated press) (equivalent to D_{S1} in Fig. 37)

GTO_1: Fast-switching GTO whose turn-on characteristic mainly determines the turn-off-stress in the DUT (equivalent to GTO_1 in Fig. 37)

C_S: Snubber capacitor, initially charged to V_{DC} (equivalent to C_S in Fig. 37)

L_σ: Stray loop inductance (≈ 200 nH)

R_2, L_1, C_1, Th and R_3 generate the forward current (10-150 A) in the DUT before GTO_1 is fired.

The test circuit (Fig. 39) simulates the upper switch of Fig. 37. The DUT forward current I_F is set to between 10 A and 150 A (type specific) to represent the worst case with regards to oscillations or snap-off. GTO_1 which triggers the diode turn-off is chosen for its fast turn-on performance and operated at room temperature. The diode to be tested is clamped in a heated press and the measurement is normally made at 110 °C. The DC-link voltage is 4000 V maximum. At the time being, all free-floating snubber diodes are routinely measured for go/no go by means of this test equipment. Any oscillating or snappy diodes are identified and scraped.