SECTION 2

PRODUCT DESIGN

BY NORBERT GALSTER
SVEN KLAKA
ANDRÉ WEBER

PRODUCT DESIGN

2.1 GTOs

The gate turn off thyristor (GTO) is a very high power semiconductor switch, destined for use in industrial applications demanding the ultimate in voltage blocking and current carrying capabilities. As a member of the thyristor family, the GTO is basically a four layer three junction regenerative (n^+pnp^+) structure. GTOs differ from conventional thyristors, in that they are designed to turn-off when a negative voltage is applied to the gate electrode, thereby causing a reversal of gate current. As a result, it is unnecessary to reverse the anode voltage to effect turn-off, so the costly commutation circuits associated with ordinary inverter grade SCRs are not required, and turn-off is much faster. During conduction, on the other hand, the device behaves just like a classic thyristor, with electrons being injected from the cathode emitter n^+, and holes from the anode emitter p^+ into the bulk of the device. The resulting plasma density is extremely high, which bestows on the GTO a very low on-state voltage, not unlike that of a diode. To optimise current turn-off capability, the gate-cathode junction must be highly interdigitated (Fig. 1). A 3000 A GTO is composed of up to 3000 individual cathode segments which are accessed via a common gate contact. Like all bipolar devices, the GTO is a current-controlled device imposing certain demands on its gate drive circuitry. A relatively high gate current is needed to turn off the device, with typical turn-off gains being in the range of 4-5.

Several different varieties of GTO are currently manufactured. Devices which have reverse blocking capability equal to their forward voltage ratings are called *symmetric GTOs*. However, most products on the market today feature an anode junction incapable of blocking reverse voltage. In this case, reverse voltage is governed by gate-cathode junction avalanche, which usually occurs around 20 V. These devices, which can sustain current in the reverse direction for short periods of time, are categorised as *asymmetric GTOs*. R*everse conducting* types constitute the third family of GTOs. Here, a GTO is integrated together with an antiparallel freewheeling diode onto the same silicon wafer.

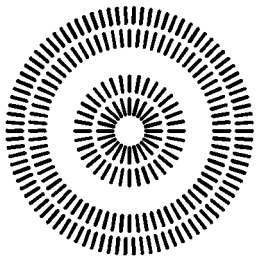

Fig. 1 The cathode of a GTO thyristor is strongly interdigitated. The most popular design features multiple segments, arranged in concentric rings around the device centre. The common gate contact can be in the centre of the device, or in a ring.

2.1.1 Two-transistor Model

The monolithic pnpn structure of either a classic thyristor or a GTO can be conceptualised as comprising an npn transistor and a pnp transistor, interconnected as shown in Fig. 2. Here, the collector of the npn transistor provides base-drive to the pnp, while the collector of the pnp, along with any externally supplied gate current, furnishes base current to the npn. In this positive feedback arrangement, regeneration occurs once the loop gain exceeds one, when each transistor drives its “mate” into saturation.

Ignoring the effects of avalanche multiplication, only significant when applied anode voltage is near junction avalanche, the pnpn structure may be analysed in terms of its transistor common-base current gains α_n and $\alpha_{P,}$ and intrinsic leakage currents I_{CBO1} and I_{CBO2}:

$I_{B2} = I_K (1-\alpha_n) - I_{CBO2}$

$I_{C1} = \alpha_p * I_A + I_{CBO1}$

$I_{B2} = I_{C1} + I_G$

$I_A + I_G = I_K$

Solving these equations for I_A :-

$$I_A = \frac{\alpha_n * I_G + I_{CBO1} + I_{CBO2}}{1 - (\alpha_p + \alpha_n)} \qquad .... 1.1$$

In this equation, $(\alpha_p + \alpha_n)$ is called the *loop gain*, G.

With forward anode voltage applied, and in the absence of any external gate current I_G, the transistor alphas are both low. The denominator of Equation 1.1 approaches unity, and I_A is little higher than the sum of the individual transistor leakage currents. Under these conditions the pnpn structure is said to be in its *forward blocking* or high impedance “off” state. The switch to a low impedance “on” state is initiated simply by raising the loop gain to one (1). Inspection of Equation 1.1 shows that as G approaches unity, I_A tends to infinity. Physically, as G nears unity, the device starts to regenerate, and each transistor drives its companion into saturation.

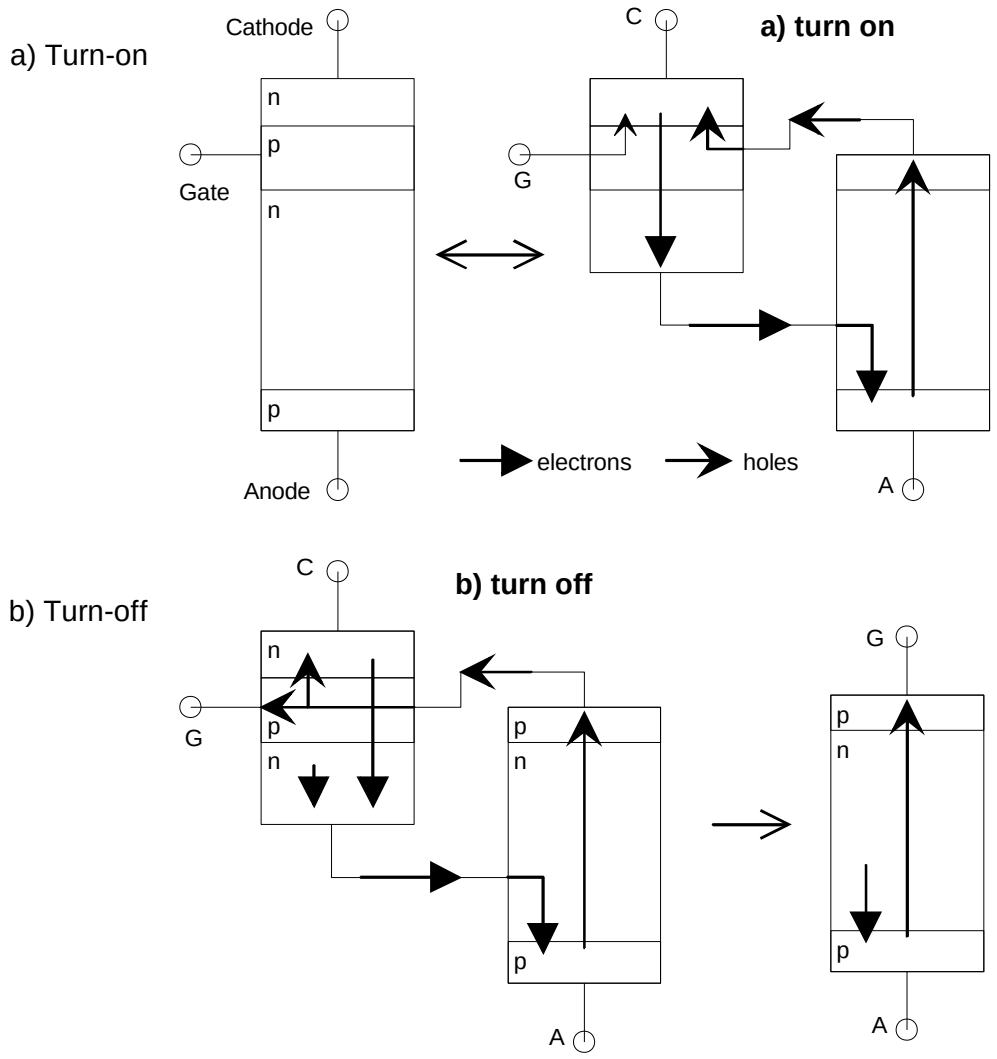

Fig. 2 Two-transistor model of a thyristor structure
a) turn-on b) turn-off

Once in saturation, all junctions assume a forward bias, and total potential drop across the device approximates that of a single pn junction. Anode current is limited only by the external circuit.

In practice, G can be boosted to unity either by raising anode voltage until avalanche multiplication occurs, or by increasing gate current. In silicon transistors, α is quite low at low emitter currents, but increases rapidly as emitter current rises. Any mechanism which causes a momentary increase in emitter current can therefore be used to turn the device on. Normally, this is done by injecting current into the p-base region via the external gate contact (Fig. 2a). Once the device has been “latched “ on in this manner, external gate current is no longer required to maintain conduction, since the regeneration process is self sustaining. Reversion to the blocking mode occurs only when anode current falls below a “holding” level, where G < 1.

2.1.2 GTO Structure

A cross section through a single GTO segment is given in Fig. 3. Typically, a cathode segment has a length of about 2 to 3 mm, and a width of 100 to 300 microns.

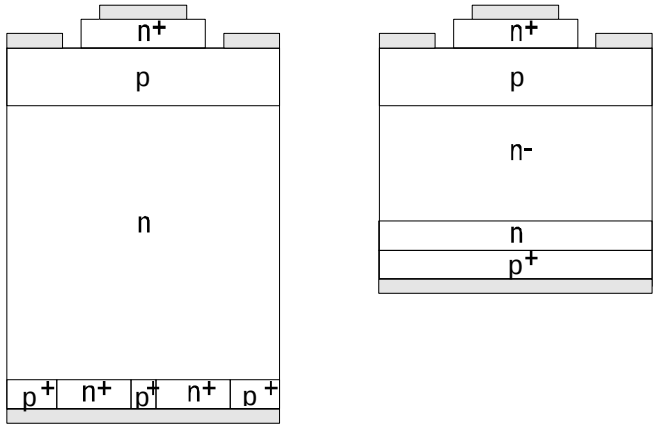

Fig. 3 Cross section through a classic anode shorted GTO, and through a buffer-layer-GTO with transparent emitter. The advantage of the buffer layer structure lies in the thinner n-base layer.

As described above, the GTO is a four layer n^+pnp^+ regenerative switching device. In order to obtain high emitter efficiency at the cathode end, desirable for good turn on characteristics, the n^+ emitter layer must be highly doped, giving a reverse breakdown voltage to the adjacent p-base of typically 20-24 V. The p-base itself, on the other hand, has conflicting requirements. Because its doping concentration is directly related to gate-cathode resistivity, and resistivity should be as low as possible to optimise the turn-off process, the doping concentration should be as high as possible. However, to obtain high emitter efficiency, the doping concentration should be low. Thus, the design of the p-base greatly influences the trade-off between turn-on and turn-off properties. In addition, the doping profile and p-base thickness play dominant roles in the voltage blocking capability of a GTO. In order to sustain forward voltages of several kV, the p-base must have a thickness in the range of a few tens of microns, and to guarantee long-term voltage-stability of the “main blocking junction” formed with the n-base “next door”, it is terminated with a negative bevel. This requires a highly graded p-base profile. The maximum forward blocking voltage of the device is always lower than the breakdown voltage of this junction, being dependent on the thickness and resistivity of the aforementioned n-region. Either the electric field at the main blocking junction reaches a critical value, or the n-base fully depletes, allowing its electric field to touch the anode emitter. The first phenomenon is called “avalanche breakdown“, the second “punch-through“. Typically, n-base thickness is around a few hundred microns.

The junction between the n-base and the p+ anode emitter is called the “anode junction“, and anode emitter efficiency is very critical to GTO design. An efficient emitter would result in a very low on-state voltage, and low gate trigger-current. However, turn-off capability of such a GTO would be poor, with very low maximum turn-off current and high losses. To explain this, the turn-off process must be examined in detail.

2.1.3 Turn-off

When the GTO is in the on-state, and then its gate is biased negatively with respect to the cathode, holes from the anode are extracted from the p-base, through the gate metallisation into the gate contact. The resultant voltage drop in the p-base above the n-emitter starts to reverse bias the gate-cathode junction, and electron injection ceases here. This process originates at the periphery between p-base and n-emitter segments and that part of the cathode still injecting electrons shrinks, as more and more of the p-base is depleted. Holes from the remaining conducting zones must then travel further laterally through the p-base to reach the gate contact. Anode current is crowded into higher and higher density filaments in those areas most remote from the gate contacts. This is the most critical phase of the turn off process, in that rapidly rising and localised high temperature can cause device failure, unless the filaments are extinguished rapidly. The filaments may be extinguished more rapidly by applying a higher negative gate voltage, but the maximum is limited by gate-cathode breakdown. As the final filaments disappear, electron injection stops completely, and depletion layers start to grow on both gate-cathode junction and forward blocking junctions. At this point, the device once again starts to support forward voltage. However, although the cathode current has ceased, anode to gate current continues to flow, as carriers from the n-base plasma diffuse into the main junction depletion layer. This “tail current”, as it is called, then decays exponentially as plasma concentration is reduced by recombination. However, because tail current is flowing while anode voltage is already high, power losses can be quite substantial. Only when tail current has completely disappeared does the device regain its steady state blocking characteristics. The presence of “free carriers” in the depletion region during the tail phase, moreover, also distorts the electric field in the depletion region associated with turn-off. The gradient of this field is in fact increased beyond that predicted from base region doping levels, and as a consequence, the maximum value reached during turn-off can in some cases exceed the avalanche limit. Resulting impact ionisation can then precipitate device failure. This phenomenon is called “dynamic avalanche”, and is one of the two principal failure mechanisms associated with power semiconductors in general.

There are three main approaches to reduce turn-off losses generated during the tail current phase, and it is desirable to combine some of these methods to achieve an optimum compromise between turn-on and turn-off performance.

Firstly, a reduction of carrier lifetime near the anode, using heavy metal diffusion or irradiation, with heavy particles like protons or helium ions, leads to a fast reduction of plasma density in the quasi-neutral part of the n-base. The advantage of this method is that reverse blocking devices can be obtained. Secondly, anode shorts can be introduced, creating a path for electrons to leave the n-base in a less restricted manner. Thirdly, a thin low efficiency emitter can be used. In this case, if the average free path of electrons is longer than the emitter thickness, then the electrons have a substantial probability of crossing the emitter into the metallic contact.

2.1.4 Turn-on

In the forward blocking state, a negative DC-voltage is applied between gate and cathode. A space charge layer extends from the blocking junction into both p- and n-base regions. However, large parts of both bases remain quasi neutral, when the applied anode voltage is lower than the maximum allowable blocking voltage. If the voltage between gate and cathode is now reversed, a current starts to flow from gate to cathode. Electrons are injected from the cathode into the p-base. As minority charge carriers, they diffuse slowly, and take a long time to cross the thick quasi neutral part of the p-base into the space charge region. This time is called “base transit time“. In the n-base, electrons are majority charge carriers and move rapidly to the anode. At first, most electrons leave the n-base through anode shorts, or cross the transparent emitter without the injection of too many holes. However, as anode current increases, a voltage drop starts to build up over the anode emitter, and hole injection accelerates. These holes must first transit the n-base before reaching the space charge layer, where they then drift towards the p-base, contribute to npn base current, and so stimulate regenerative action. However, considerable time is needed for these holes to move just from the anode to the n-base. Before this happens, electrons arriving in the n-base from the cathode, via the p-base, modulate the electric field and reduce the width of the depleted region. This leads to an increase in the time required for holes to cross the n-base. Secondly, holes are less mobile than electrons, and they drift slowly. During the period when electrons alone contribute to current flow, anode current is already substantial, causing a marked drop in anode-cathode voltage. It can take a long time, in the order of ten microseconds, for the anode-cathode voltage to drop to its final on-state value, and for free carrier densities to reach equilibrium. During this period, the GTO can be latched locally, while other parts remain in a transistor-like mode. This leads to uneven current distribution over the silicon wafer, hence to local heating. To ensure a fast and homogeneous turn-on, both the amplitude and rise time of the gate trigger current should be as high as possible. This speeds up npn transistor turn-on, and promotes fast decay of anode voltage.

2.1.5 Anode-Shorted GTOs

As mentioned above, to improve the GTO's turn-off properties, anode shorts are incorporated, to provide a path for electrons to reach the contact metallisation, without the injection of holes. However, during turn-on, these anode shorts cause a substantial increase in gate trigger current, I_{gt}. The reason is, that substantial anode current can flow through the shorts, without generating sufficient voltage drop over the anode emitter to inject holes.

2.1.6 New Technology

The ability of buffer layers to increase the blocking voltage of power devices has been known for a long time. The merit of such $n^+pn^-np^+$ or n^+pinp^+ structures is, that the field is stopped in the n layer, permitting the field shape to be trapezoidal, rather than triangular. Device thickness can then be drastically reduced, with commensurate improvements in both on-state and dynamic losses. However, the incorporation of buffer layers into GTOs created difficulties in the past. The major shortcoming was that the high conductivity buffer layer, juxtaposed between anode and n-base, increased the efficiency of the anode shorts during turn on. Electrons transiting through the n-base were collected in the buffer layer, and then flowed laterally along the anode junction to reach the shorts. Because the voltage drop was lower than in a comparable structure without buffer, the density of anode shorts had to be reduced to ensure good turn-on properties. This in turn degraded turn-off performance, and reduced the margin for reasonable compromise between turn-on and turn-off properties. To overcome this difficulty, ABB Semiconductors developed the concept of a buffer layer, combined with a thin low efficiency anode emitter. The design of this so called *transparent emitter* is such, that electrons have a high probability of crossing the emitter without stimulating the injection of holes. Thus, there is no need to incorporate anode shorts to decrease turn-off losses. The major benefit of this technology, is to marry low turn-off losses with low gate trigger currents. During turn-on, the anode current at which hole injection starts is not defined by a lateral voltage drop, as it is for an anode shorted GTO. During turn-off, electrons are not confined in the n-base, so the tail current time is very short.

2.1.7 RC-TGTOs

In the past, most GTOs, unlike diodes, had no buffer layer. This meant that a GTO wafer was much thicker than a comparably rated diode wafer. Because the overall thickness of an RC-GTO is determined by the thicker device, the design of the diode section was far from ideal, and the benefits expected from monolithic integration were compromised by high diode losses. ABB's transparent emitter technology, on the other hand, permits the integration of a free-wheeling diode (with acceptable losses) and a GTO on the same wafer.

A second problem was, that since both GTO and diode shared a common blocking junction, gate current could flow through the common p-base into the anode of the diode, unless precautions were taken to prevent this. Such a path is a short circuit to gate current, in that the anode of the diode and the cathode of the GTO are at the same potential. Two approaches have been proposed to circumvent this, both introducing impedance between the GTO p-base and the diode. Firstly, a groove can be etched into the p-base or, alternatively, the p-bases can be separated by a small n-conducting region (Fig. 4). The advantage of the latter technique is that current flowing from GTO gate to the diode is attenuated by a p-n junction, which does not present ohmic resistance to gate current.

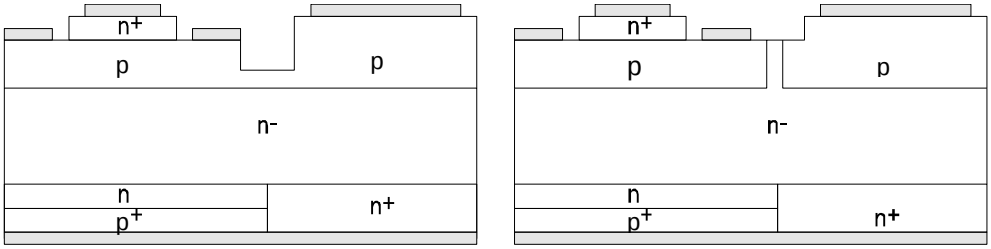

Fig. 4 Comparison of resistive separation with pnp separation of a GTO and integrated freewheeling diode. The advantages of the pnp separation are very low gate leakage currents, and high blocking stability.

2.1.8 Turn-off of a Complete GTO

While turn-off of a single GTO segment is well understood, the turn-off of a complete device is much more difficult to grasp. The reason is the in-homogeneous nature of the process in a large GTO. Segments close to the gate contact tend to turn-off first, while those remote from this contact must contend with the negative feedback introduced by metallisation and p-base lateral resistance. As gate current flows horizontally through these elements, it creates a degenerative voltage drop. During turn-off then, those parts of the GTO remote from the gate are still conducting, while other parts closer to the gate are already turned off. The blocking junction, in the vicinity of the turned off segments, is already supporting voltage. Load current is restricted to those areas still in conduction, and current density in these regions will increase. As mentioned earlier, this “filamentation“ is the second main culprit of device destruction, after dynamic avalanche. In most applications, a turn-off snubber is specified to limit dv/dt reapplied to the device. The maximum turn-off current of a GTO depends a great deal on the snubber capacitance chosen, and on stray inductance in the snubber network. Of course, the aim is to minimise snubber capacitance for cost reasons.

In practice, the aim of the manufacturer is to augment GTO turn-off capability through improved device homogeneity. However, inherent obstacles, like voltage drop in the gate metallisation, set limits on what can be done.

A breakthrough can be achieved by using a low inductance gate driver. With this technique, the device is turned off rapidly, with electron injection over the entire cathode ceasing, before voltage starts to rise over the main blocking junction. In this way, filamentary turn-off is avoided. Such a device is called a “Gate-Commutated Thyristor“, or *GCT*.

2.2 IGCTs Integrated Gate-Commutated Thyristors

The fundamental difference between a conventional GTO and the GCT lies in the very low inductance gate driver system, inherent to the GCT. Ultra low inductance has been achieved, through the development, by ABB, of a new optimised housing and integrated gate driver concept. The complete switch, comprising a GCT married to its low inductance gate drive unit, is named *IGCT*, for “Integrated Gate-Commutated Thyristor“.

2.2.1 Hard Turn-off

As described above, a fundamental difference exists between a GTO and the GCT in the turn-off process. In the GCT, or IGCT, the entire anode current is commutated from cathode to gate in a very short time. Since the npn-transistor is inactive thereafter, the pnp-transistor is deprived of base-current, and turns off. The GCT, therefore, turns off in a transistor mode, thus completely eliminating the current filamentation problems inherent in conventional GTOs. Additional advantages are a dramatic reduction of storage time to less than 2µs, and a reduction in fall time to around 1µs. Thus, the series connection of GCTs is facilitated, compared to GTOs, by the very low dispersion associated with these times.

The key to achieving “hard” turn-off of this nature, is the duration of the time interval in which it occurs.

The gate-cathode junction must be reverse biased before any voltage rise of the p-base to n-base junction occurs.

ABB Semiconductors' GCTs are designed to allow a time duration of 1 µs for current commutation, which implies:

$$\mathbf{di_{gqm}/dt > I_{tgq}/1\mu s\ (A/\mu s)}$$

Fig. 5 depicts a simplified schematic of the gate circuit. For cost effectiveness, the voltage sourcing the turn-off process should not exceed the maximum gate-cathode breakdown voltage. Because the gate inductance of a classic 5" GTO-housing is around 40 nH, the turn-off capability of a 5" packaged GCT would be limited to less than 1000 A.

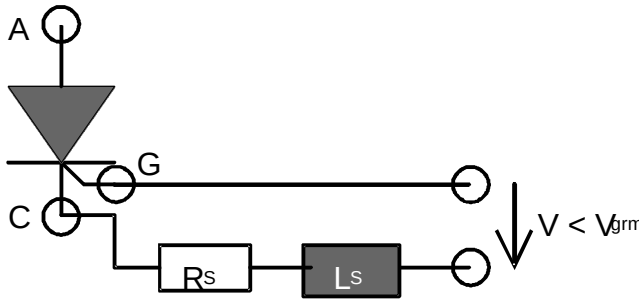

Fig. 5 Simplified schematic of a gate circuit for turn-off

This leads to the conclusion that, in order to yield creditable switching performance, special housings with total gate inductance below 3nH are indispensable. To achieve this, gate connection through the ceramic housing is realised by a concentric copper disc, which behaves as an ultra-low-inductance strip line. The gate ring itself is contacted by twelve copper strips, running in grooves machined in the copper cathode pole-pieces (fig. 6). Thanks to this concept, the gate inductance of an ABB GCT is as low as 2.7 nH.

When the companion gate driver is connected directly to the GCT, total parasitic gate-circuit inductance is still no more than 3.5 nH.

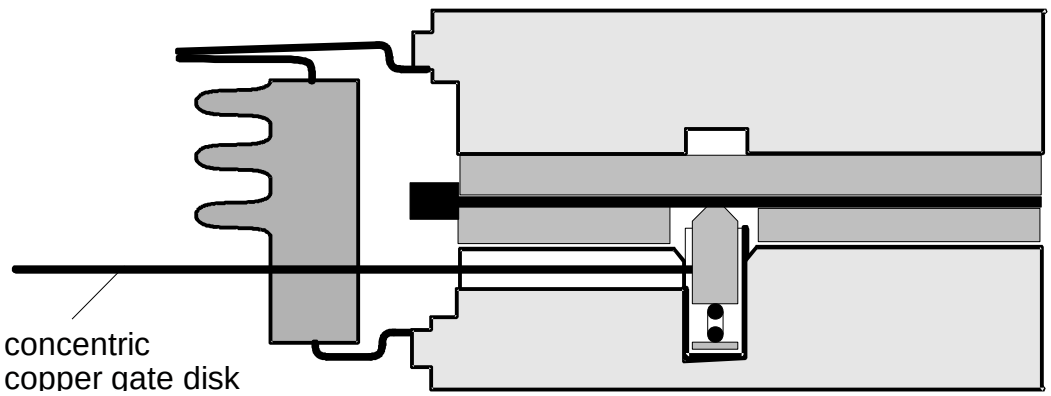

Fig. 6 Low inductance gate contact of the GCT

2.2.2 Snubberless Switching

As turn-off is achieved in a *transistor* mode, the current remains homogeneous throughout switching, and there is no need to restrict reapplied dv/dt. Fig. 7 illustrates a circuit that permits snubberless operation of the switch. Typical plots of current and voltage during turn-off are shown in Fig. 8. About 1 µs after activating the gate driver, anode-voltage starts to rise. Once this voltage has reached the dc-link voltage, anode-current commutates from the GCT to the free-wheel diode. Voltage overshoot is dependent on stray inductance, circuit di/dt, and the forward recovery voltages of the free-wheel and clamp diodes. Unclamped stray inductance should be kept below 300 nH. Due to the very low storage and fall times, the minimum off-time can be reduced below 10µs.

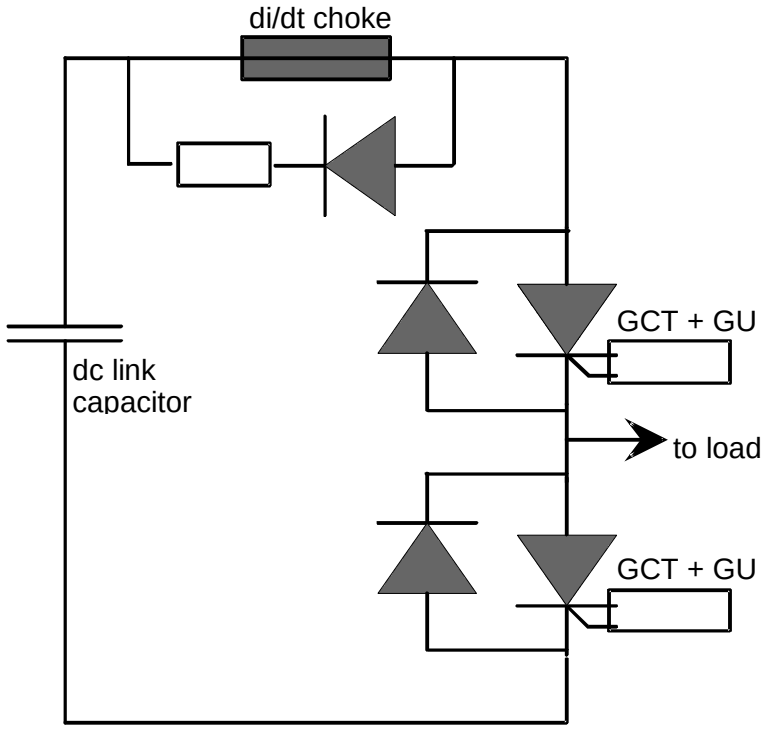

Fig. 7 Application example for snubberless operation of the IGCT

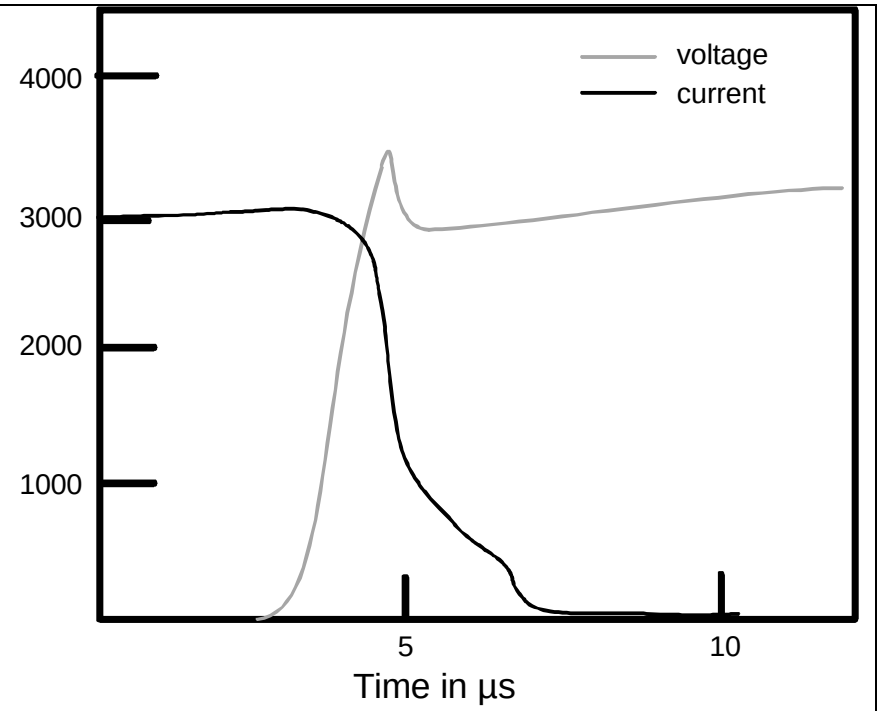

Fig. 8 Typical turn-off waveforms of an IGCT

The tail-current of a GCT lasts for but a few microseconds, thanks to the advanced transparent emitter concept, which authorises a narrow n-base. Of course, this new device may also be operated with a snubber.

When so equipped, due to the homogeneous turn-off process, the GCT is endowed with a much higher turn-off capability than a comparable GTO. For example, a 4.5 kV GCT, rated for snubberless switching at 3 kA, can easily turn off 5 kA with a 4 µF snubber capacitor.

2.2.3 Turn-on

At the beginning of the turn-on process, only the npn transistor is active. With the gate forward biased, electrons are injected from the cathode, which, after a few microseconds, stimulate hole injection from the anode. This relatively slow regenerative process normally limits the current rise, that can be achieved by ordinary GTOs. The low inductance gate circuit of a GCT, on the other hand, allows very high turn-on currents with fast rise times. This maintains the GCT in its transistor mode during the turn-on process, when current ramps of several kA/µs are readily achievable, with perfectly homogeneous current distribution. Of course, if favourable for the application, a GTO-like turn-on mode can also be implemented.

The energy consumption of the GCT + gate-driver pair (IGCT) is much lower than that of a conventional GTO, thanks to the modest backporch requirements and reduced tail-current of the transparent emitter/ buffer layer design. Furthermore, although the unity-gain peak gate-current is 3 or 4 times higher than for a GTO, the storage time is 15 to 20 times shorter resulting in an overall reduction of gate charge to start-of-tail by a factor of about 5.

2.3 Diodes

In all GTO or IGCT applications, high performance diodes are a must. As the performance of GCTs improves, the pressure increases for corresponding advances in diode behaviour.

2.3.1 Commutation Behaviour of Diodes

The diodes specified for fast switching GTO, GCT or IGBT applications, must feature not only low static and dynamic losses, but must also demonstrate exemplary recovery behaviour. In most applications, the critical need to minimise stray inductance between switch and associated snubberless diode, encourages super-fast diode commutation. Such commutation places a premium on low reverse peak current I_{rr}, and "soft recovery" performance.

In order to achieve "soft recovery" it is necessary that, at the instant of maximum reapplied voltage, sufficient carriers remain available to support the required "tail current".

To obtain a low reverse recovery peak, the flooded pn junction must be rapidly depleted.

Several methods are available to achieve these aims:

1) Provision of a sufficiently thick n-base, to provide a diffusion current through the remaining neutral zone, once the maximum voltage has been reached, plus the reduction of lifetime to reduce I_{rr}.
2) Introduction of an n-buffer layer to serve as a carrier reservoir, together with low lifetime and/or shallow anode diffusion profiles.
3) Carrier control, by modifying the emitter efficiency on the anode side.
4) Carrier control, by local lifetime control.

or any combination of the above.

While 1) leads to an unacceptably high on-state voltage for a given reverse recovery peak, 2) and 3) presuppose either additional diffusion or mask steps and so increase production costs significantly.

ABB Semiconductors favours local lifetime control, in order to ensure the best trade-off between on-state and dynamic losses, while maintaining ideal recovery behaviour under all conditions of operation.

2.3.2 Carrier Lifetime

In p-i-n diodes, carrier lifetime τ is usually adjusted to a low value, in order to reduce the stored charge $Q_F = \tau * i_{F,}$ for a given forward current i_F. Additionally, the recombination rate of the recovered charge Q_R during commutation, increases as τ decreases.

Conversely, the ohmic voltage drop V_F across the base region w, increases with decreasing carrier lifetime:

$V_F \sim w^2/(\mu_n + \mu_p)* \tau$,

where μ_n , μ_p represent electron and hole mobility.

This equation is valid for relatively high values of lifetime only. For lower values of τ, the dependency becomes exponential.

As a consequence, lifetime has to be adjusted in such a way that an optimum trade-off, between static and dynamic losses, is achieved.

While this can be implemented by homogeneous lifetime profiling, as produced by electron irradiation, more versatile tools are required, to shape the reverse recovery waveforms to the requirements of the particular application.

2.3.3 Carrier Lifetime Profiling

The dynamic behaviour of diodes is strongly determined by carrier distribution in the device, just prior to commutation. This distribution, in turn, is influenced by the distribution of recombination centres (traps) in the device.

In the case of homogeneous lifetime, carrier distribution, due to different hole and electron mobilities, shows a minimum close to the *mid region*, while the edge concentration of carriers on the anode side is significantly higher than that on the cathode side (Fig. 9, Curve a).

In contrast, a reverse recovery waveform with a low peak reverse current and soft recovery, is obtained by a distribution with a minimum near the *anode* (Fig. 9, Curve b) and a high concentration on the cathode side.

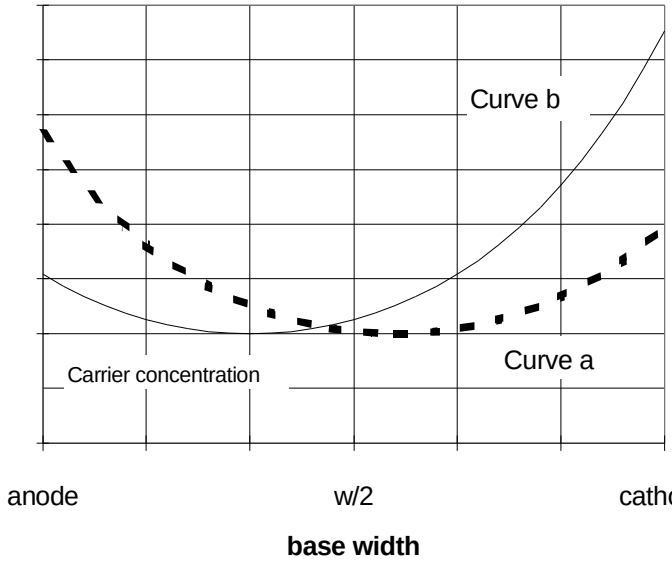

Fig. 9 On-state carrier distribution, resulting from different lifetime distributions. Curve a) for homogeneous lifetime, Curve b) for profiled lifetime.

Heavy metal diffusion and irradiation by light ions are among the many tools available, to produce the lifetime profiles required.

While heavy metal diffusion (gold, platinum) produces trap profiles that reflect the known behaviour of the particular element used, ion irradiation is more flexible. Irradiation by helium or hydrogen ions has become a popular tool for local lifetime tailoring, in high power devices. This technique is widely considered as being far superior to heavy metal diffusion for lifetime control, not only because of its high reproducibility, but also because irradiation by protons or helium ions, allows the concentration of recombination centres to be profiled in two or even three dimensions.

Furthermore, it can also be considered as a corrective tool, being an "off-line" process, routinely used after the initial device electrical evaluation that follows clean room processing. It can also be easily combined with electron irradiation.

2.3.4 Carrier Lifetime Control by Light-Ion Irradiation

Implanted high energy ions are stopped inside the target, at a depth determined by their energy. They create most lattice damage towards the end of their trajectories, leaving the bulk silicon penetrated along their paths relatively unharmed. This produces a well defined and localised damage zone, with a high concentration of defects (Fig. 10) acting as recombination centres. It is this zone that determines both carrier lifetime and carrier distribution within the device.

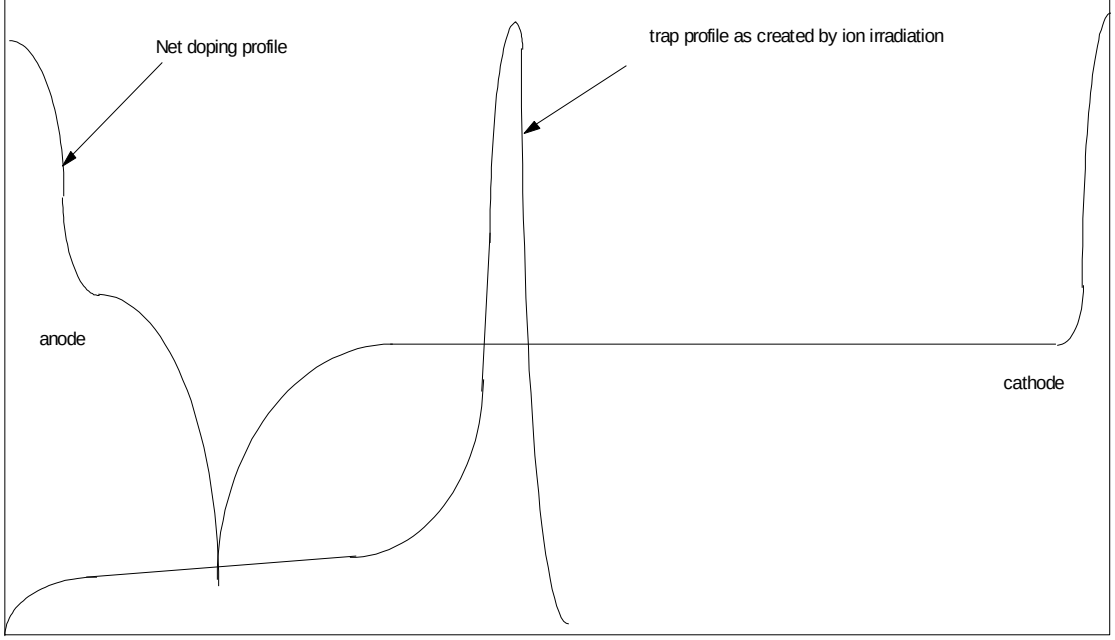

Fig. 10 Doping and trap profiles in a diode, as created by ion irradiation.

The desired defect density in this "recombination layer" can be tailored, by choice of the ion dose. Furthermore, particular defect properties may also be programmed, by post-irradiation annealing.

Device behaviour and performance, are strongly affected by the position and properties of the locally “doctored” region, with its modified lifetime. However, in combination with electron irradiation, a wide range of different ion doses and energy combinations is possible, This enables the dynamic behaviour of the device to be varied almost at will, without greatly influencing its static properties.

In the last ten years, many investigations on proton (occasionally helium) irradiation of GTOs, thyristors and diodes have been performed. While researchers have often been attracted by more exotic methods, involving complex and costly production processes, a simple approach, such as single energy single dose irradiation, has proven to be the most suitable.

2.3.5 Electrical Behaviour of Proton Irradiated Diodes

Fig. 11 compares the turn-off waveforms of a snubber diode with homogeneous lifetime (that is, a concentration of recombination centres as determined by electron irradiation), to those of a proton and electron irradiated device (5SDF 03D4501). The test circuit is given in Section 3, Figure 39. The electron irradiated diode shows severe "snap off", at a source voltage of 3.2 kV, whereas the 5SDF 03D4501 exhibits “good-natured“ (soft) behaviour, even at 3.5 kV. Also, I_{rr} of the proton irradiated diode is lower by about 30%. Silicon material and diffusion profiles are the same for both devices.

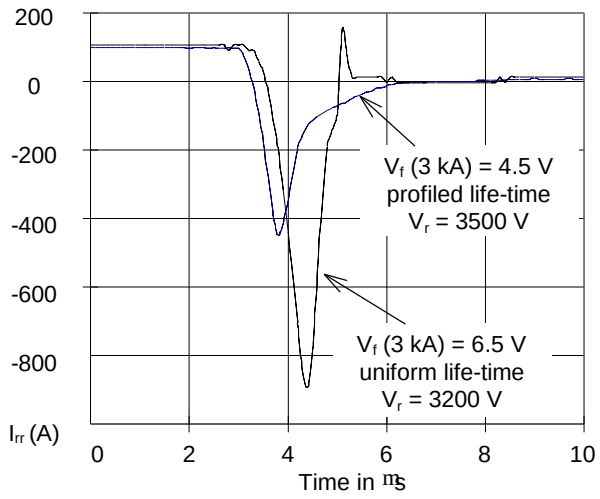

Fig. 11 Comparison of different lifetime technologies in 4.5 kV snubber diodes. Note the different source voltages.

Fig. 12 illustrates current and voltage waveforms of the same 5SDF 03D4501, turned off from an extremely low forward current density of about 1 A/cm^2, where snap-off is even more likely to occur. Even under these conditions, the device performs very well.

Table 1 is a comparison of the major characteristics of this product, with those of a gold doped and an electron irradiated diode. It shows, unequivocally, that a lower dynamic forward voltage (V_{fr}), and lower leakage current are bonus benefits of ion irradiation.

Lifetime Technology	Blocking		Turn-off @ di/dt = 100 A/us, V_{dc} = 1000 V, I_F = 1000 A			Turn-on @ 1000 A/us	
	V_F @ 3000A, 125°C	leakage current @ 4.5 kV, 125 °C	I_{rr}	Q_{rr}	s-factor	V_{fr} @ 25°C	V_{fr} @ 125°C
gold	6.5 V	24 mA	185 A	615 µC	1.2	90 V	145 V
electrons	6.8 V	6 mA	235 A	585 µC	0.7	55 V	120 V
protons	6.5 V	11 mA	175 A	620 µC	1.4	52 V	115 V

Table 1: Comparison of snubber diodes with different lifetime technologies.

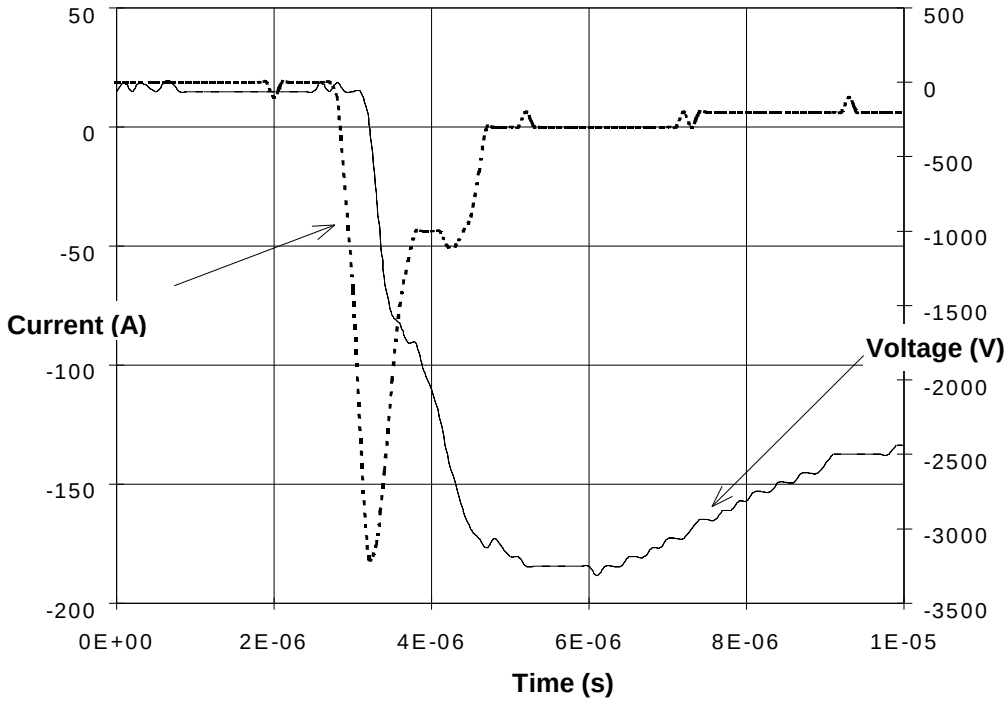

Fig. 12: 5SDF 03D4501, HH76. 31B in Undeland circuit,
I_F=10 A, V_{dc} =3500V, T=110°C

2.4 Cosmic Radiation

In the early 1990's, it was discovered that exposure to high energy cosmic particles could precipitate the random destruction of power semiconductors, subjected to high blocking voltages for long periods of time. ABB Semiconductors has carefully investigated this phenomenon, and has established design rules to minimise the possibility of failures. For each ABB semiconductor product, a failure rate due to cosmic radiation can be specified, as a function of the applied voltage.